

FIG. 1

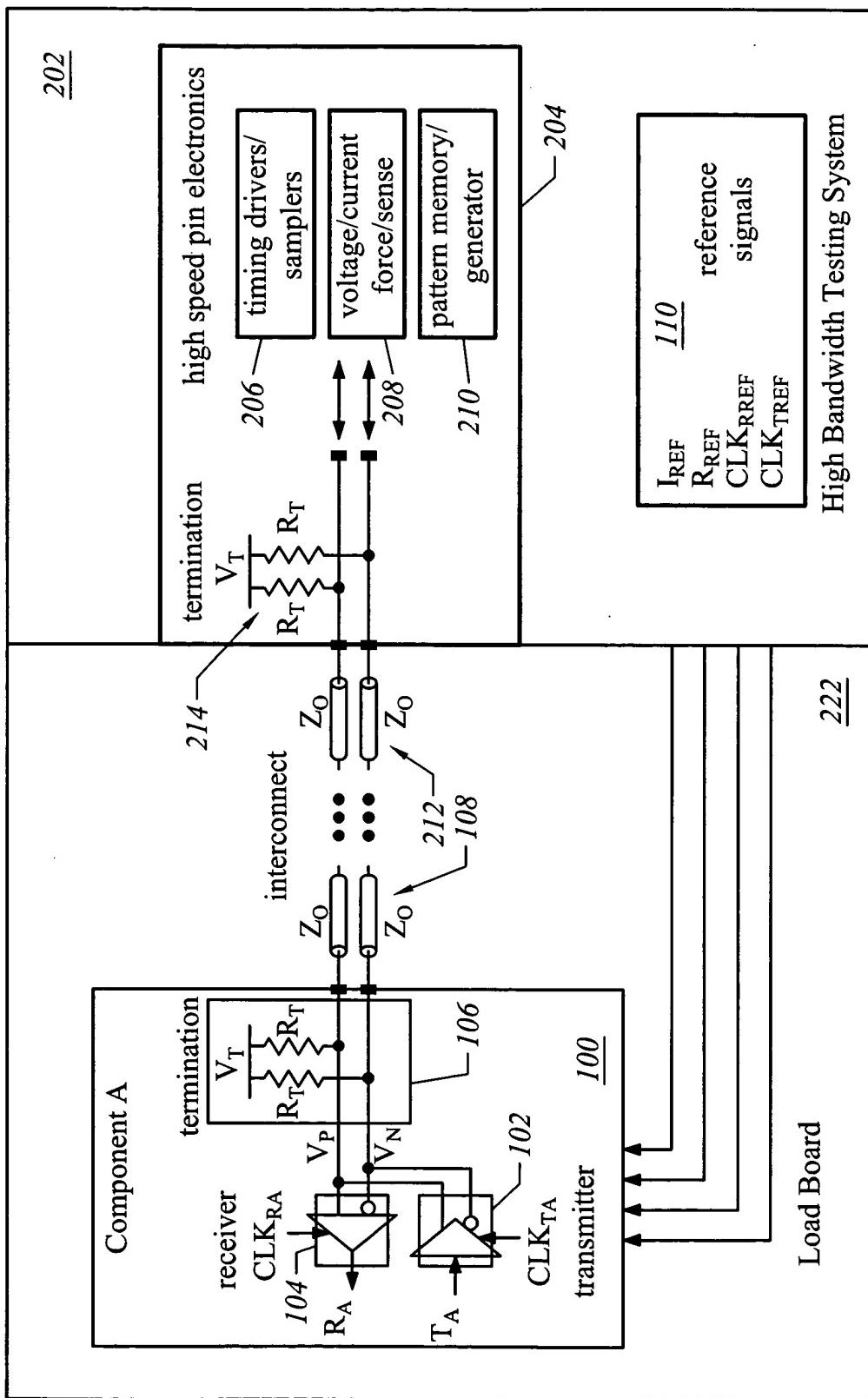


FIG. 2

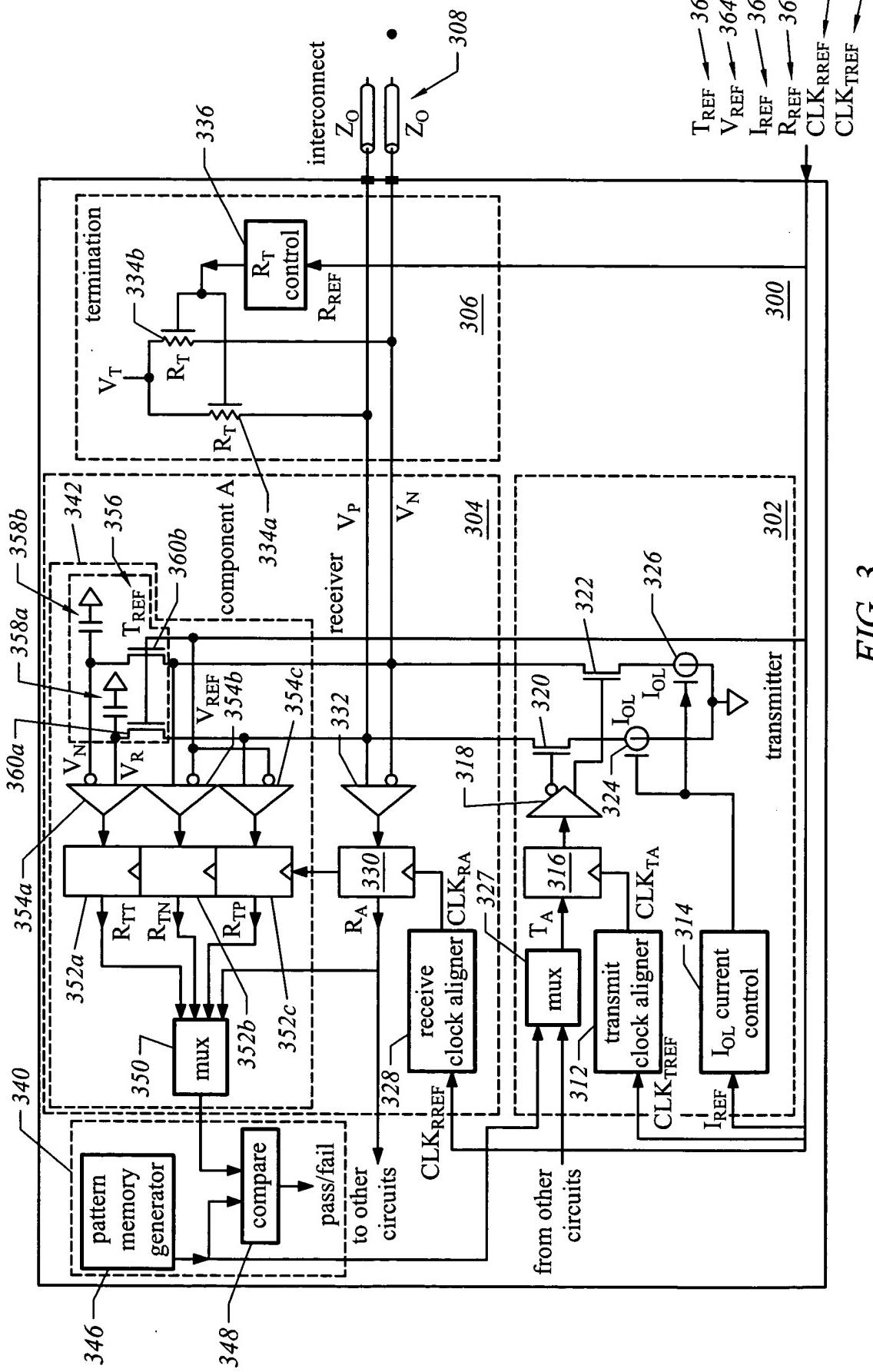
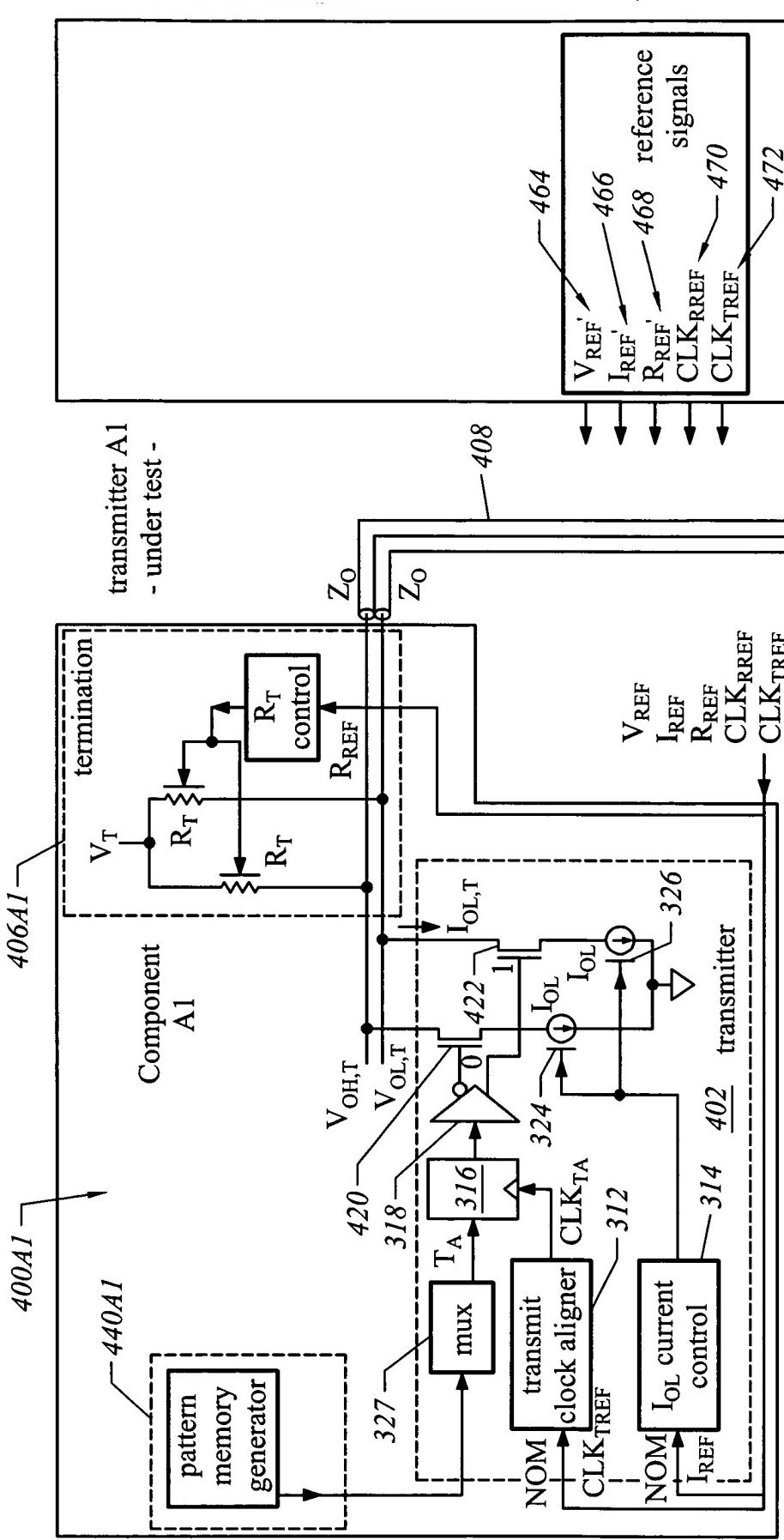


FIG. 3



(See Fig. 4B)

FIG. 4A

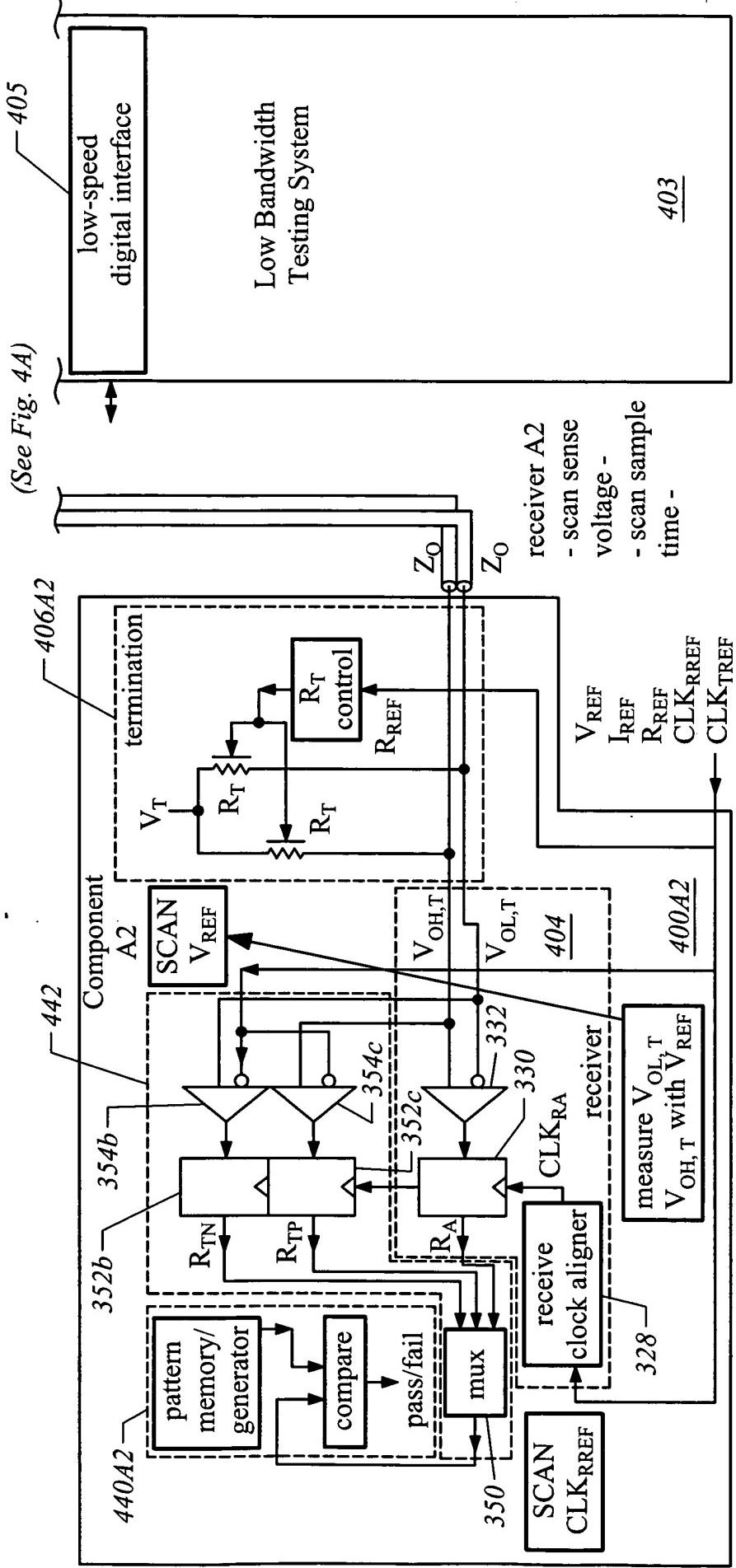


FIG. 4B

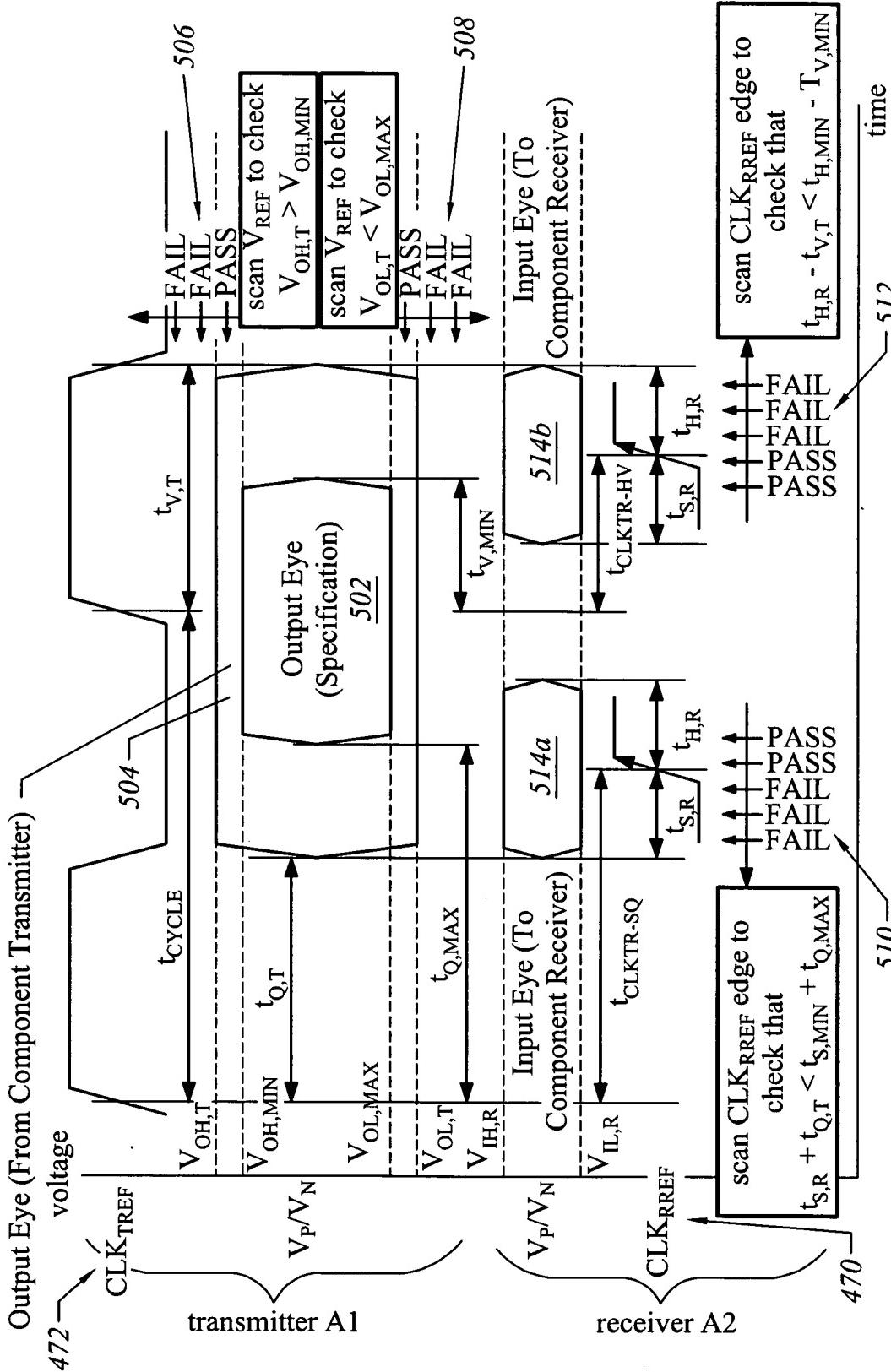


FIG. 5

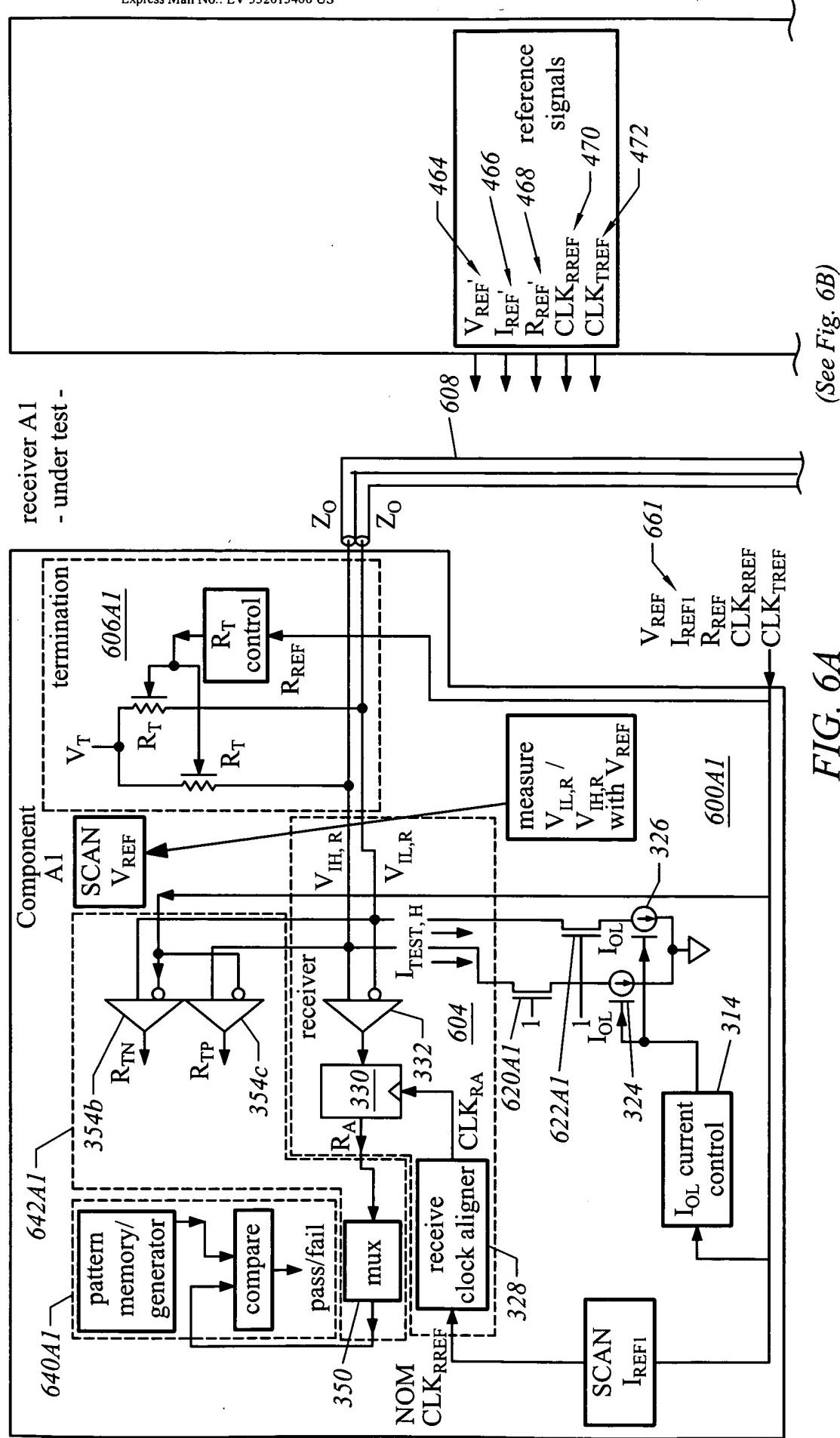


FIG. 6A

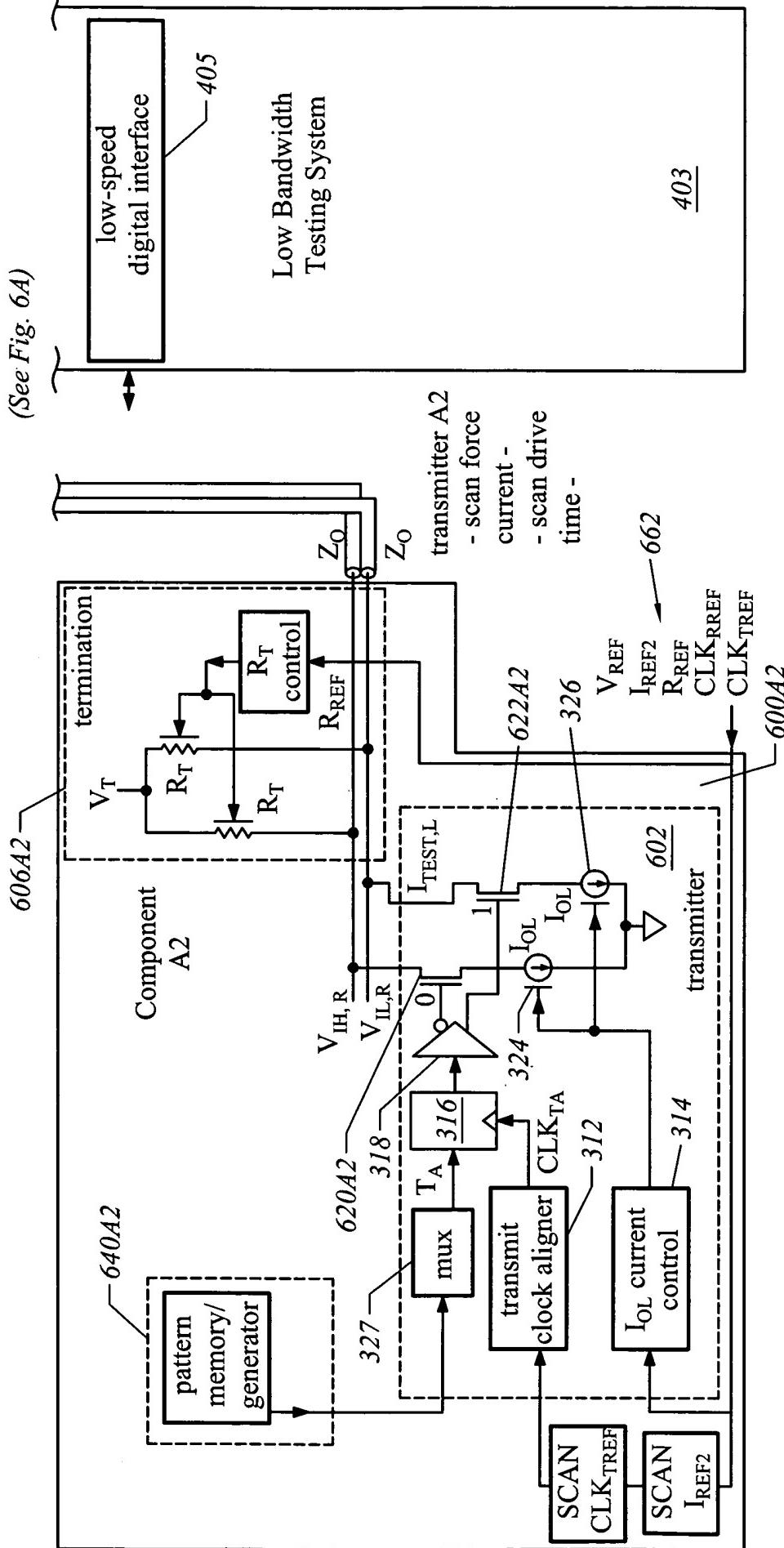


FIG. 6B

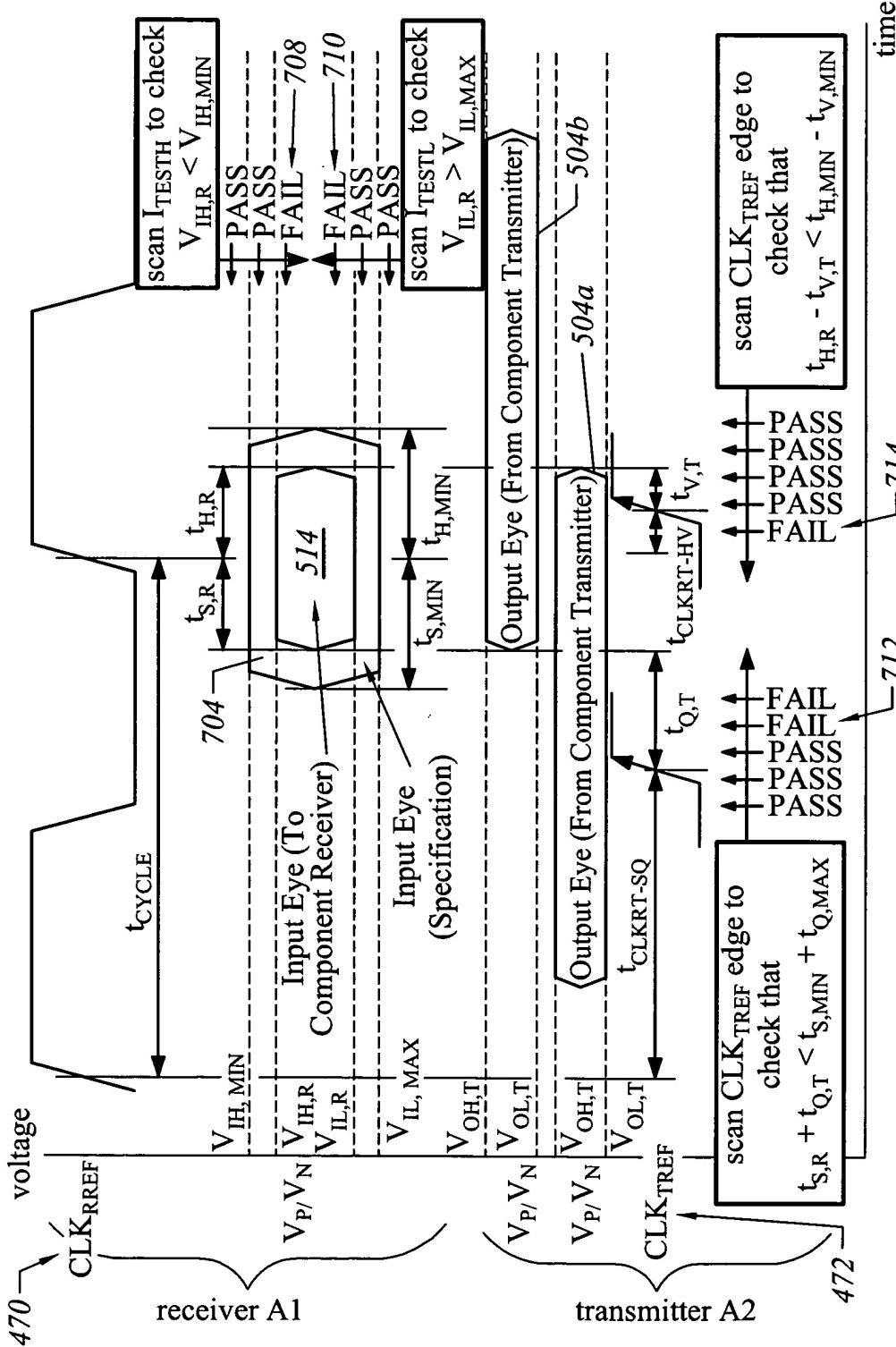
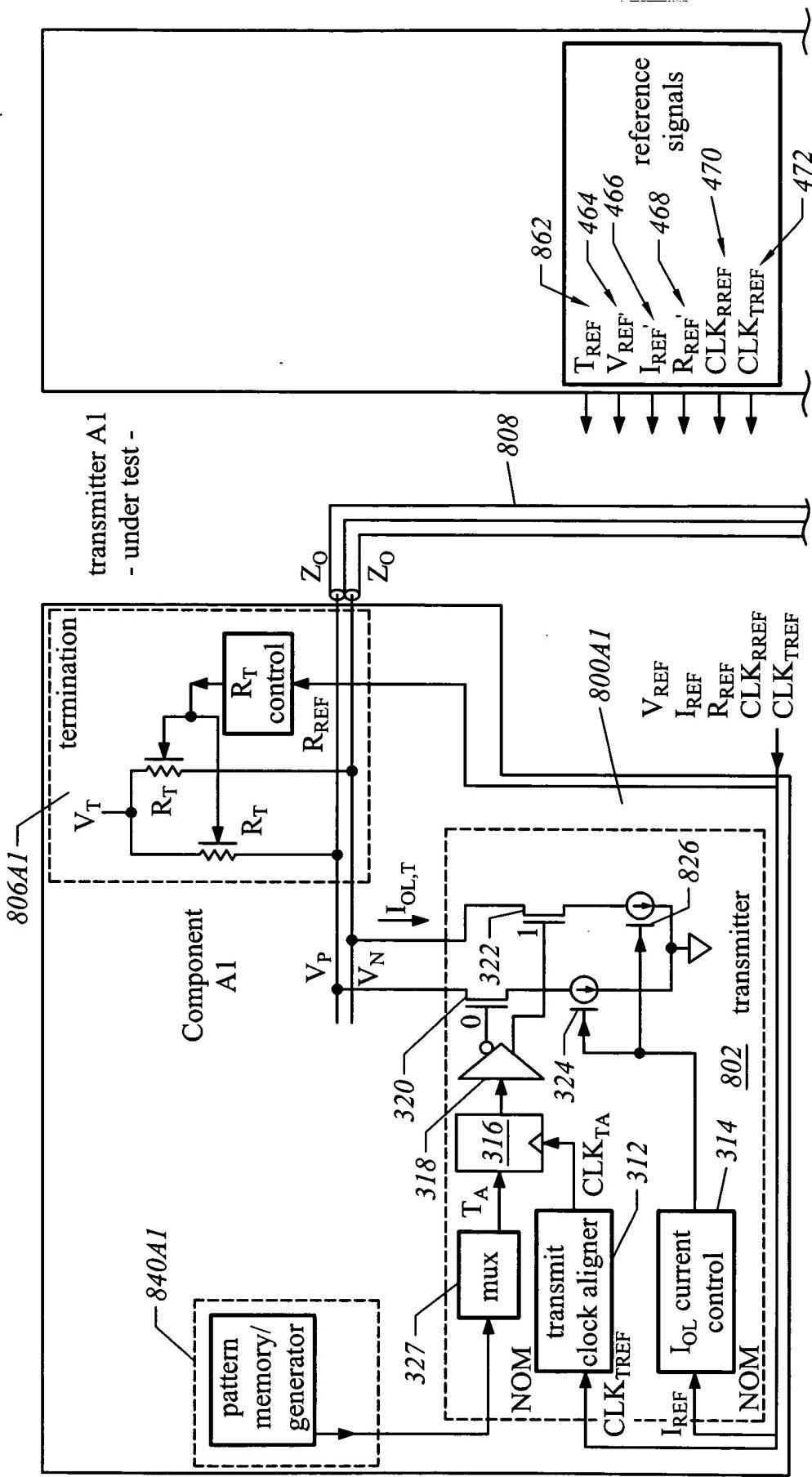


FIG. 7



(See Fig. 8B)

FIG. 8A

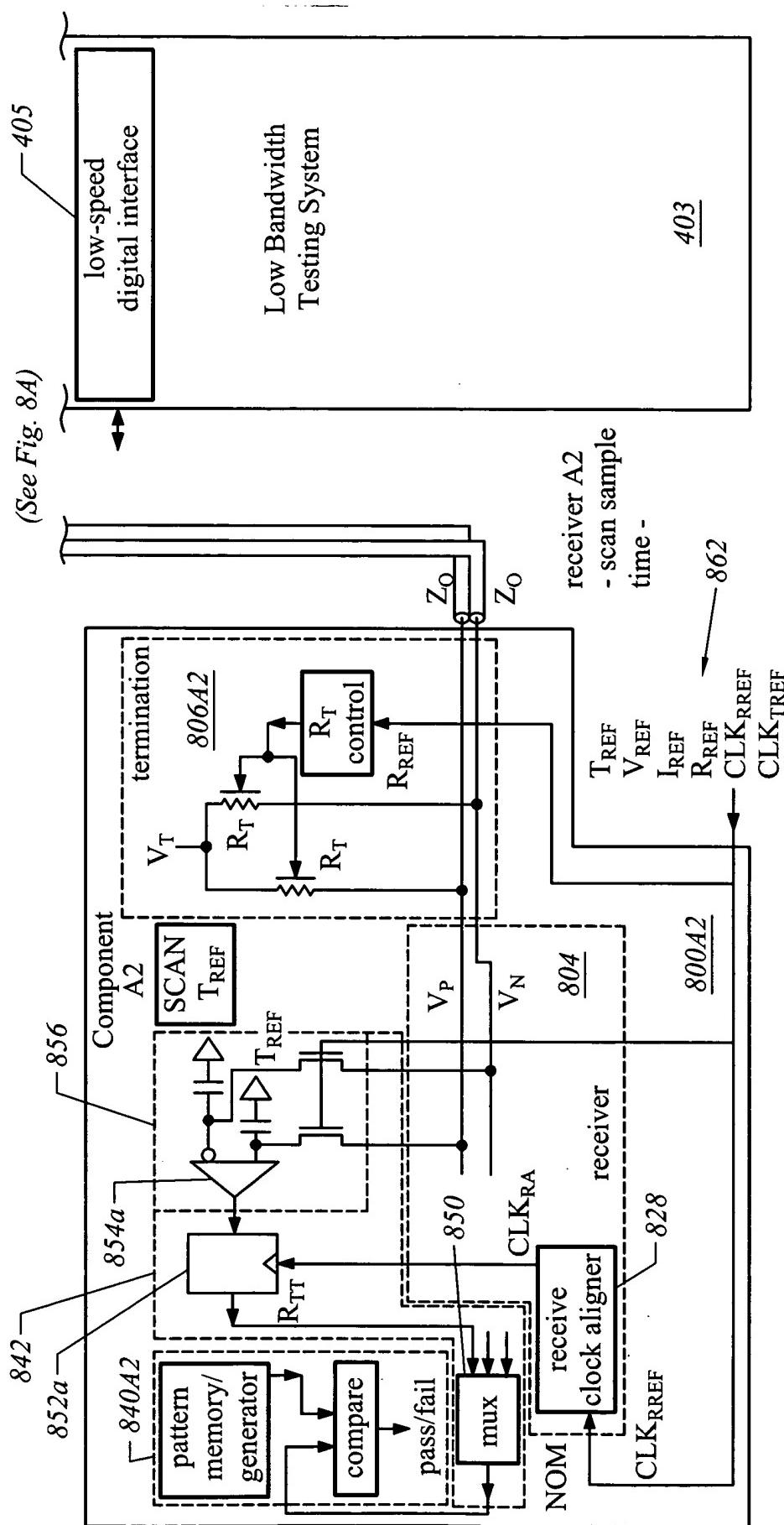


FIG. 8B

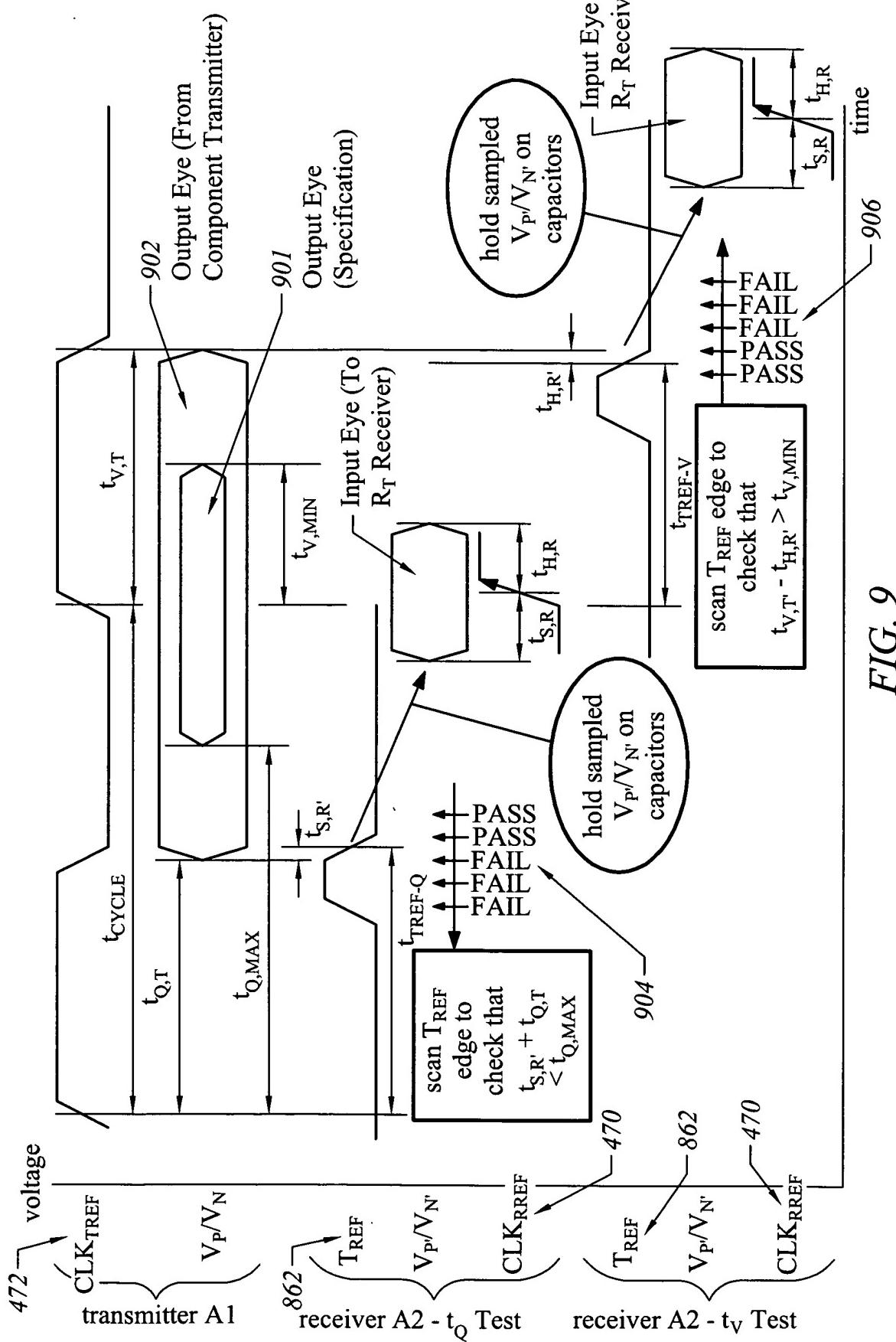


FIG. 9

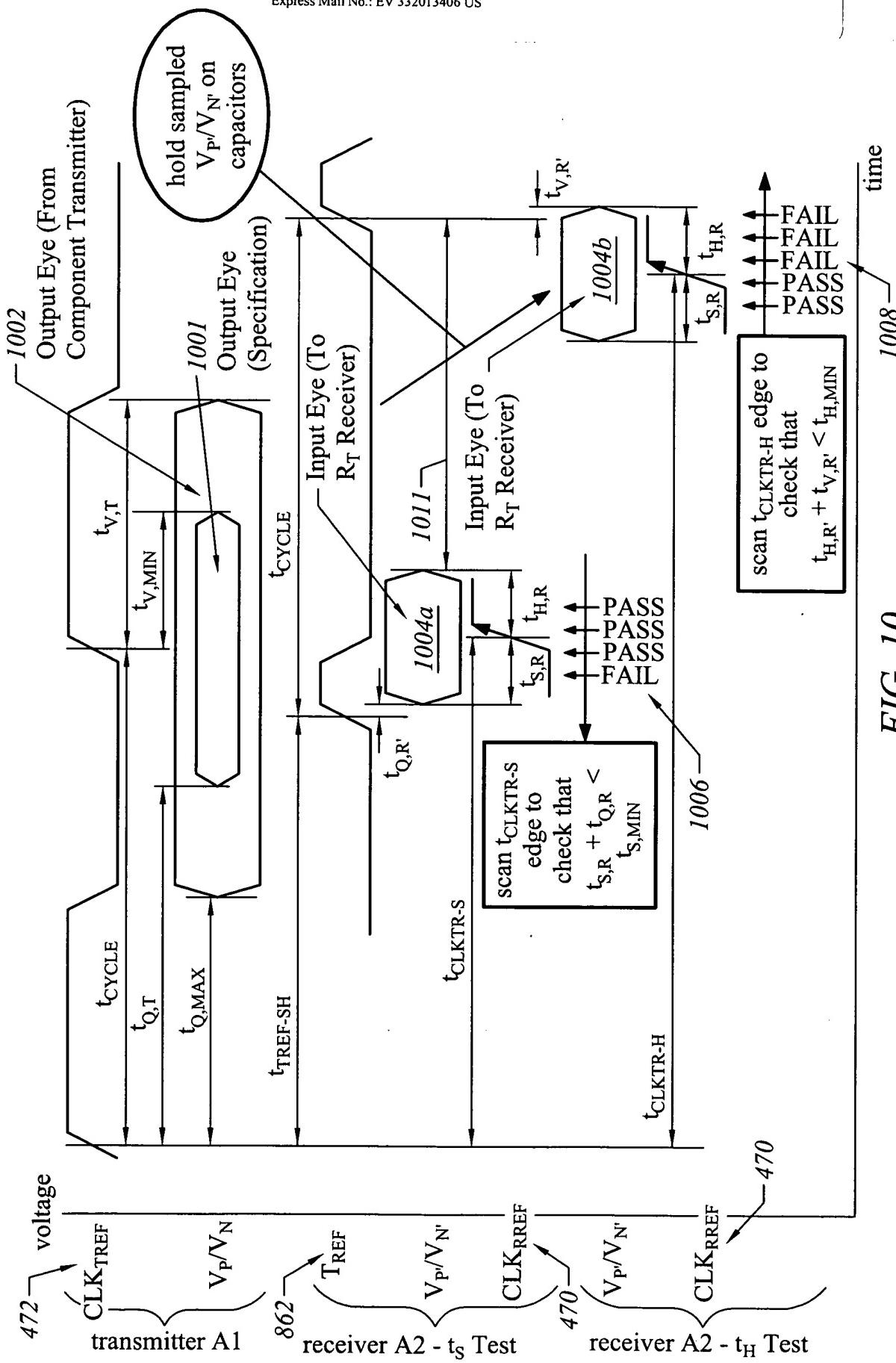


FIG. 10

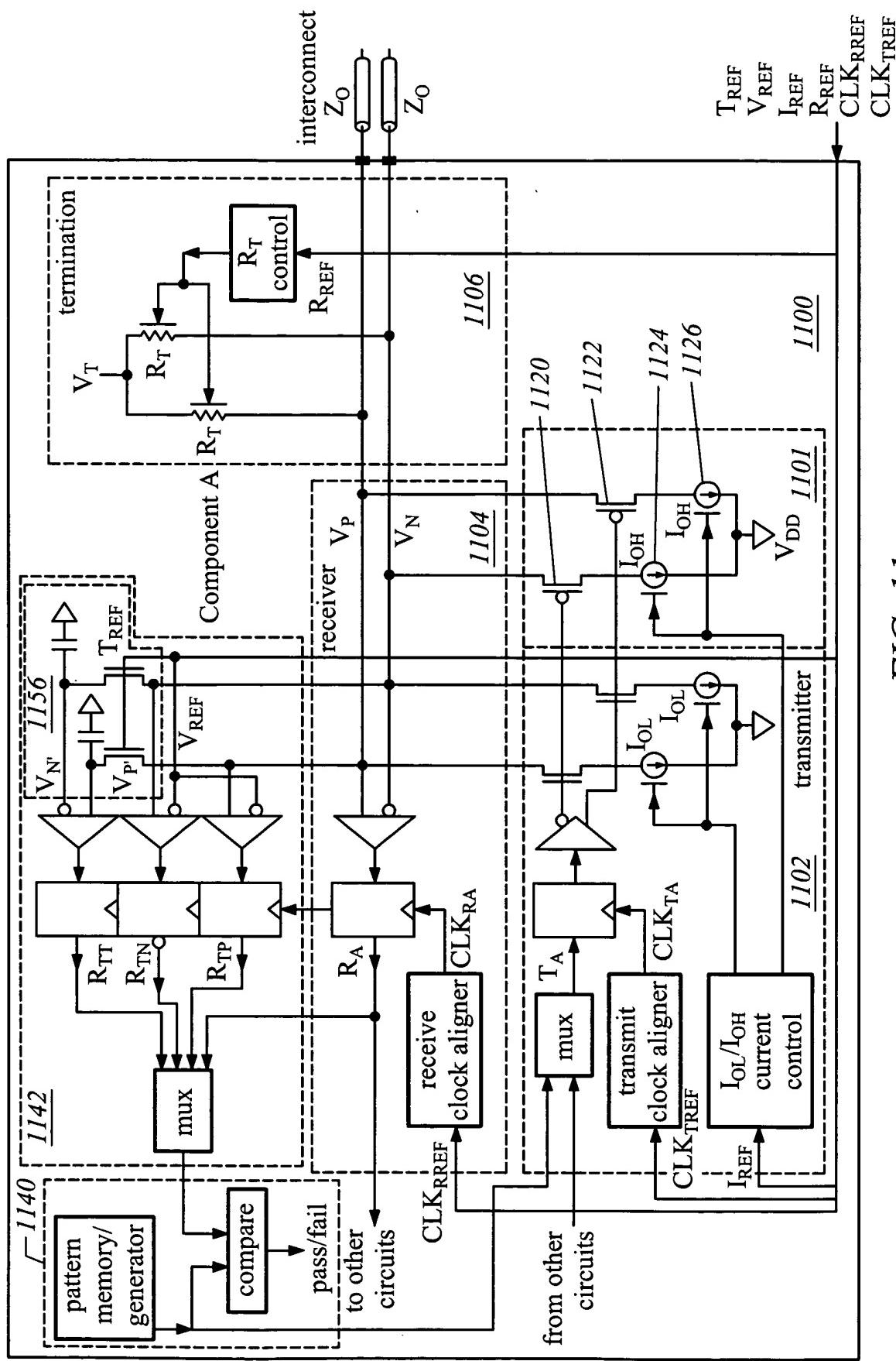


FIG. 11

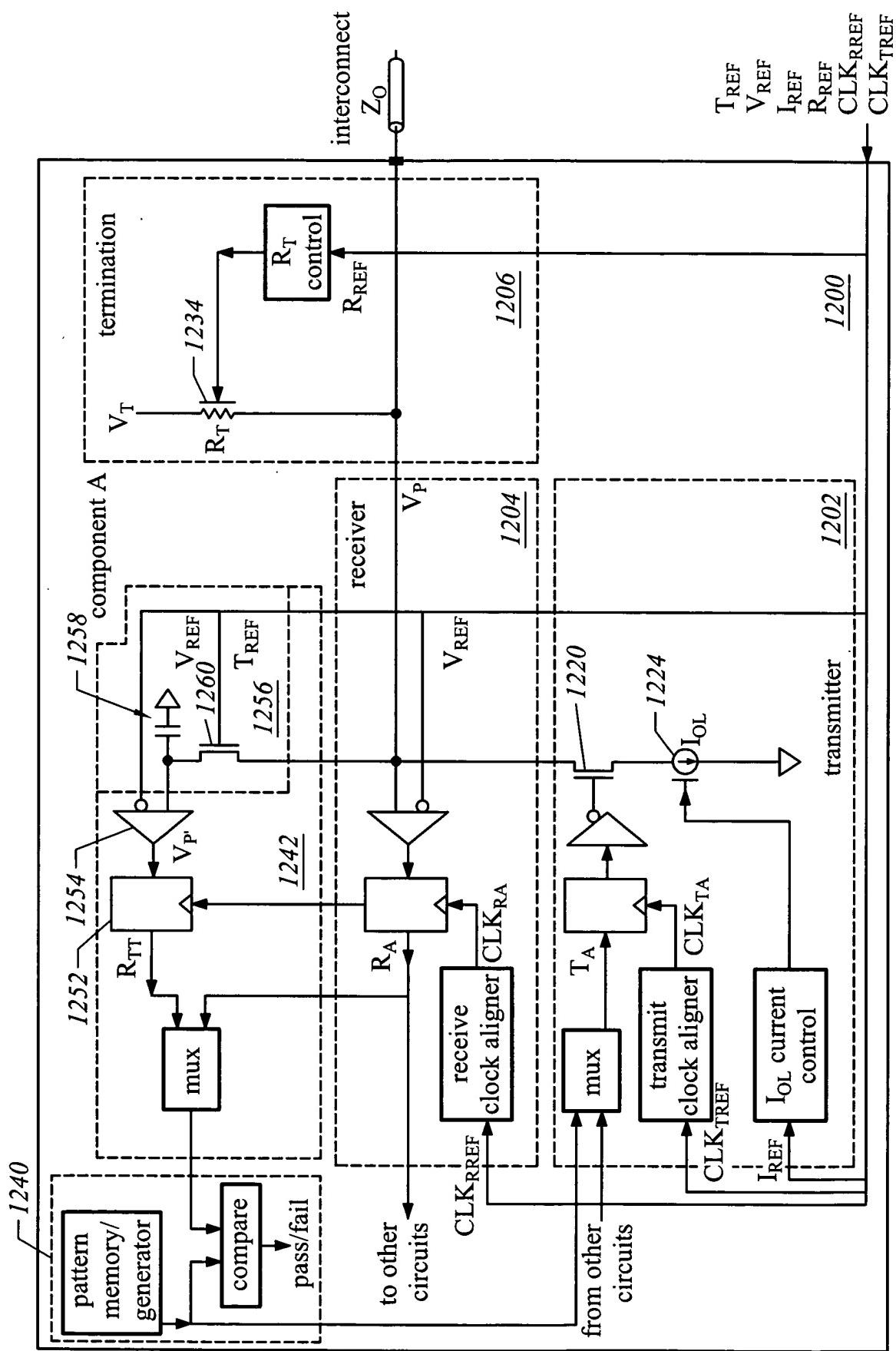
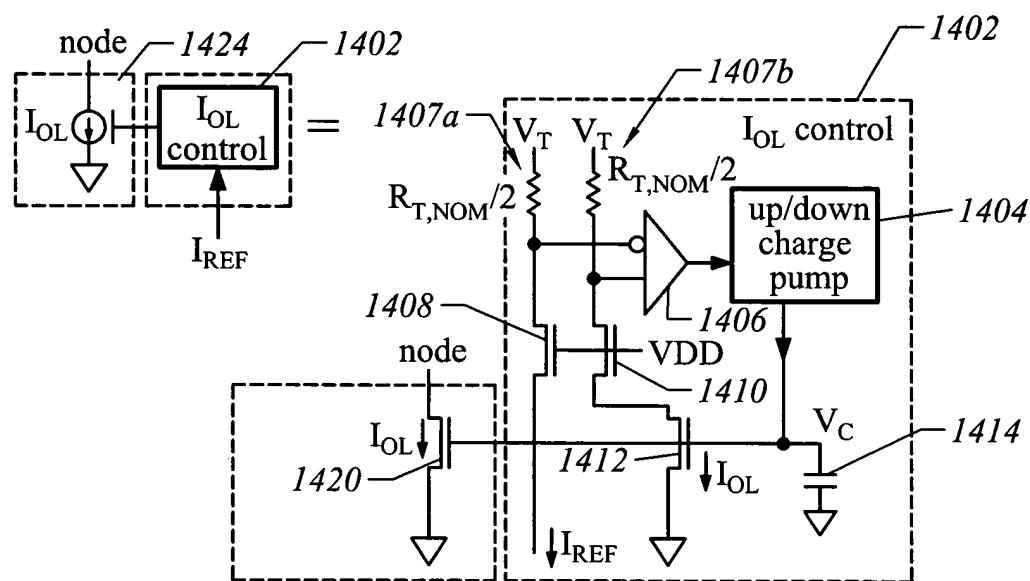
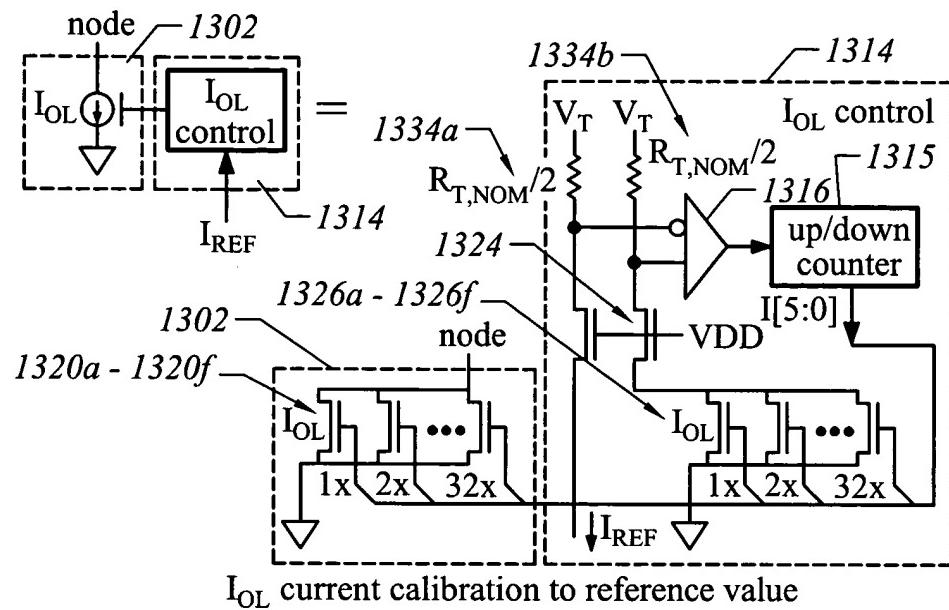
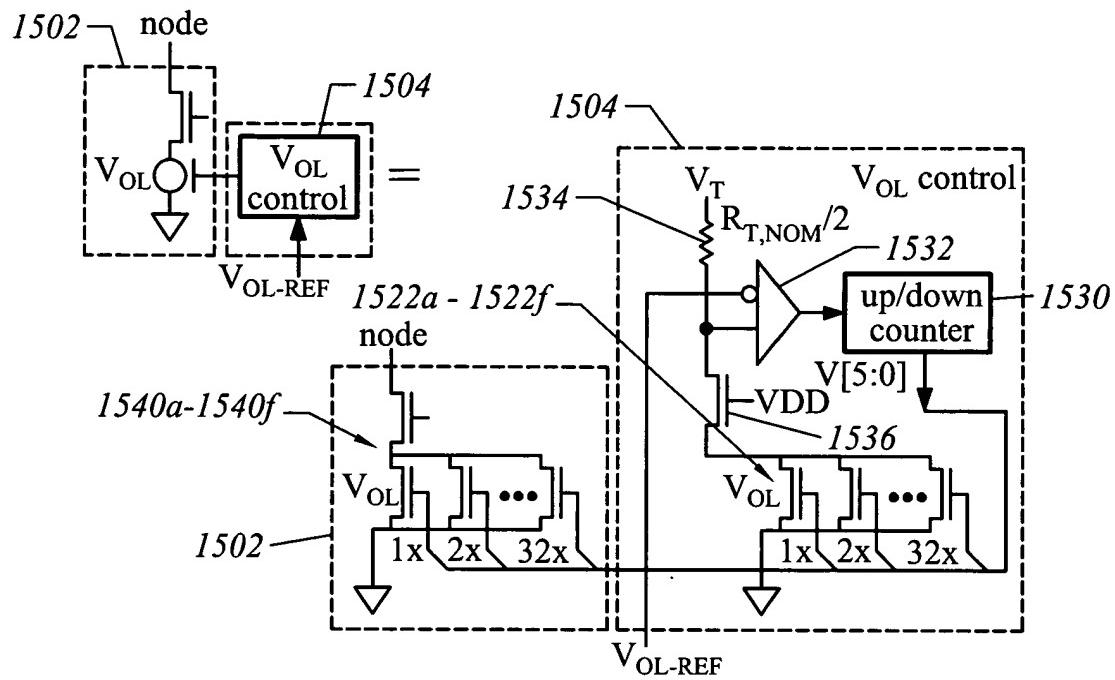


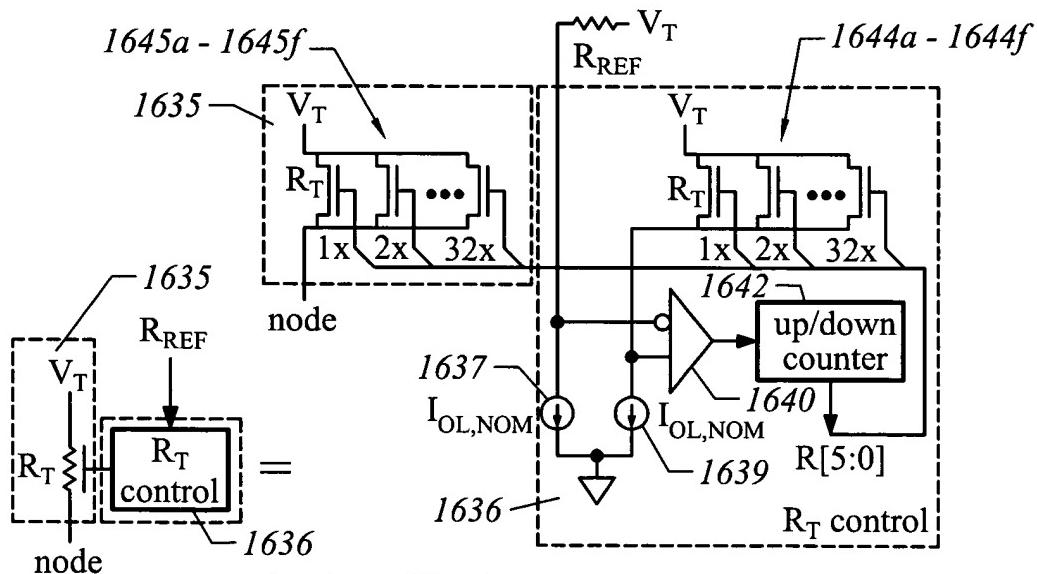
FIG. 12





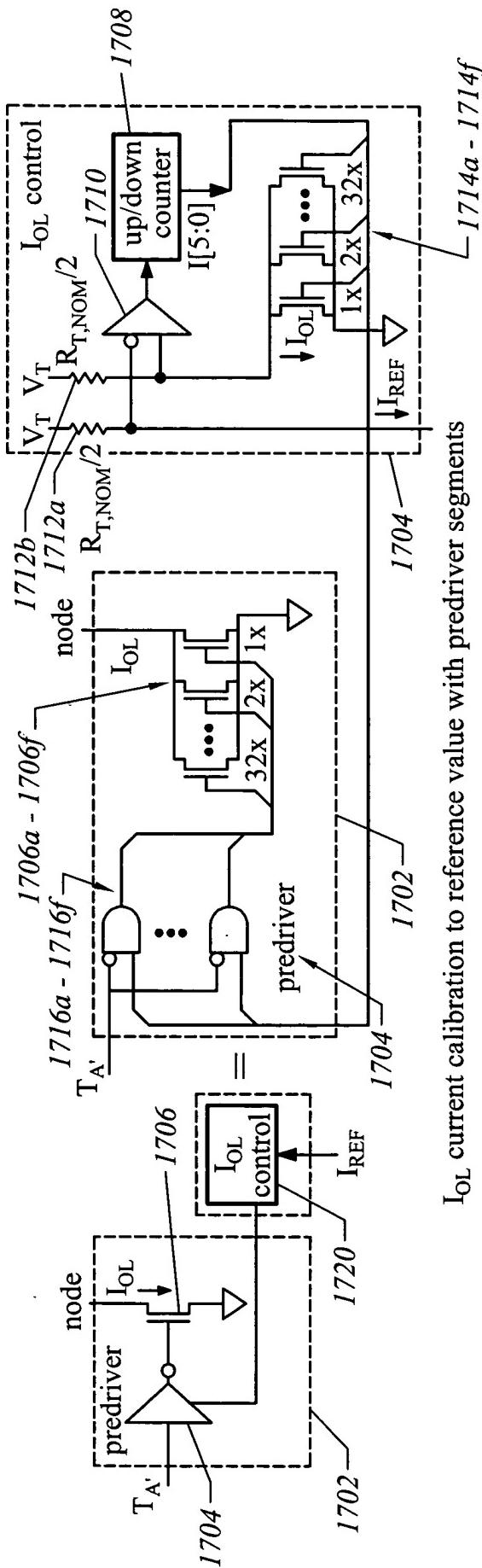
V_{OL} voltage calibration to reference value

FIG. 15



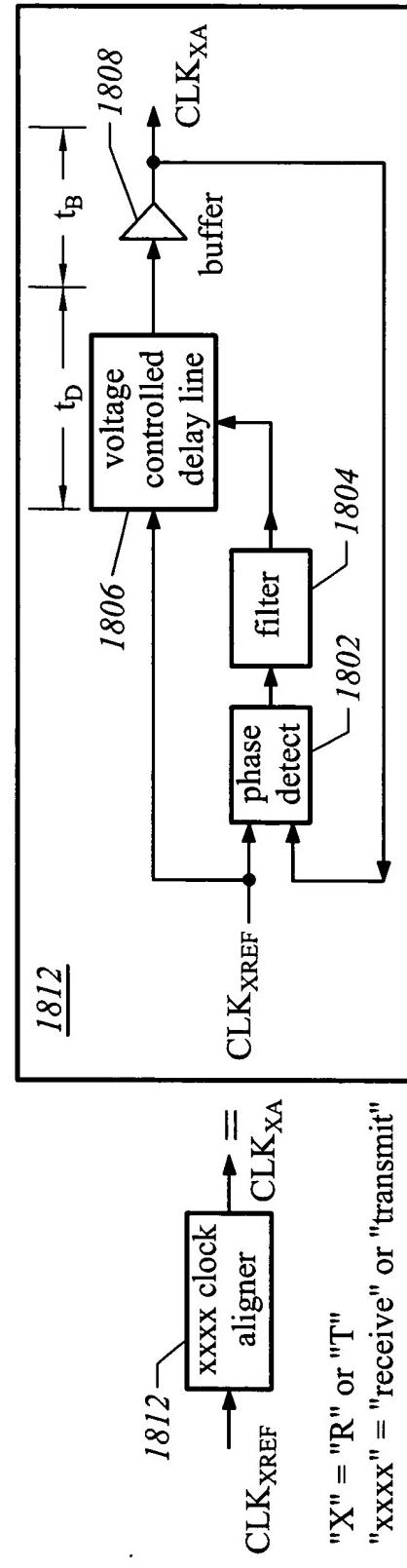
Termination calibration to reference value

FIG. 16



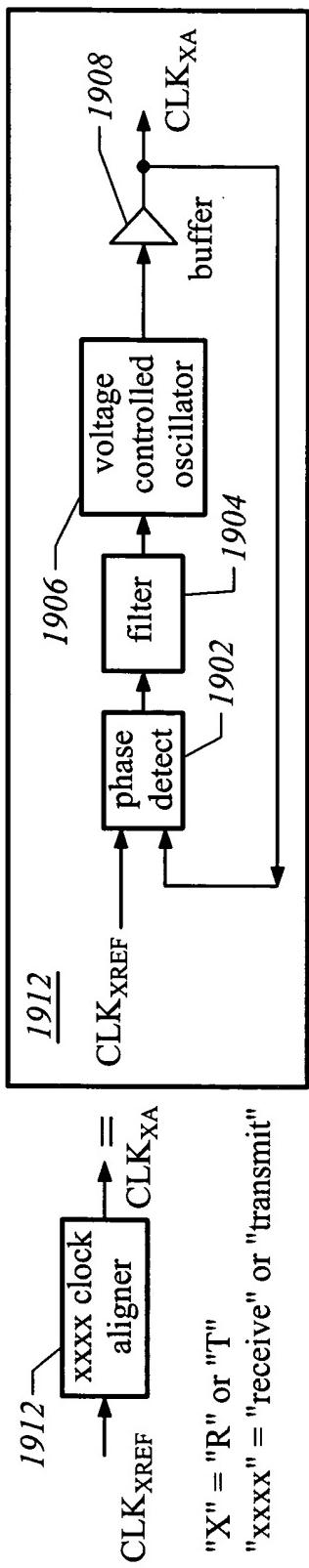
I_{OL} current calibration to reference value with predriver segments

FIG. 17



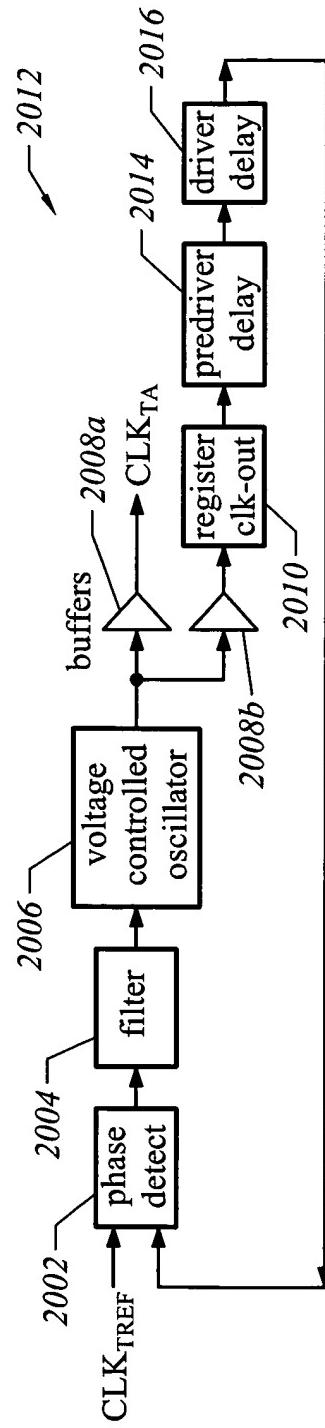
"X" = "R" or "T"
"XXXX" = "receive" or "transmit"

FIG. 18



Receive or transmit clock alignment using PLL (phase-locked-loop)

FIG. 19



Transmitter clock aligner with output register/predriver/driver loop compensation

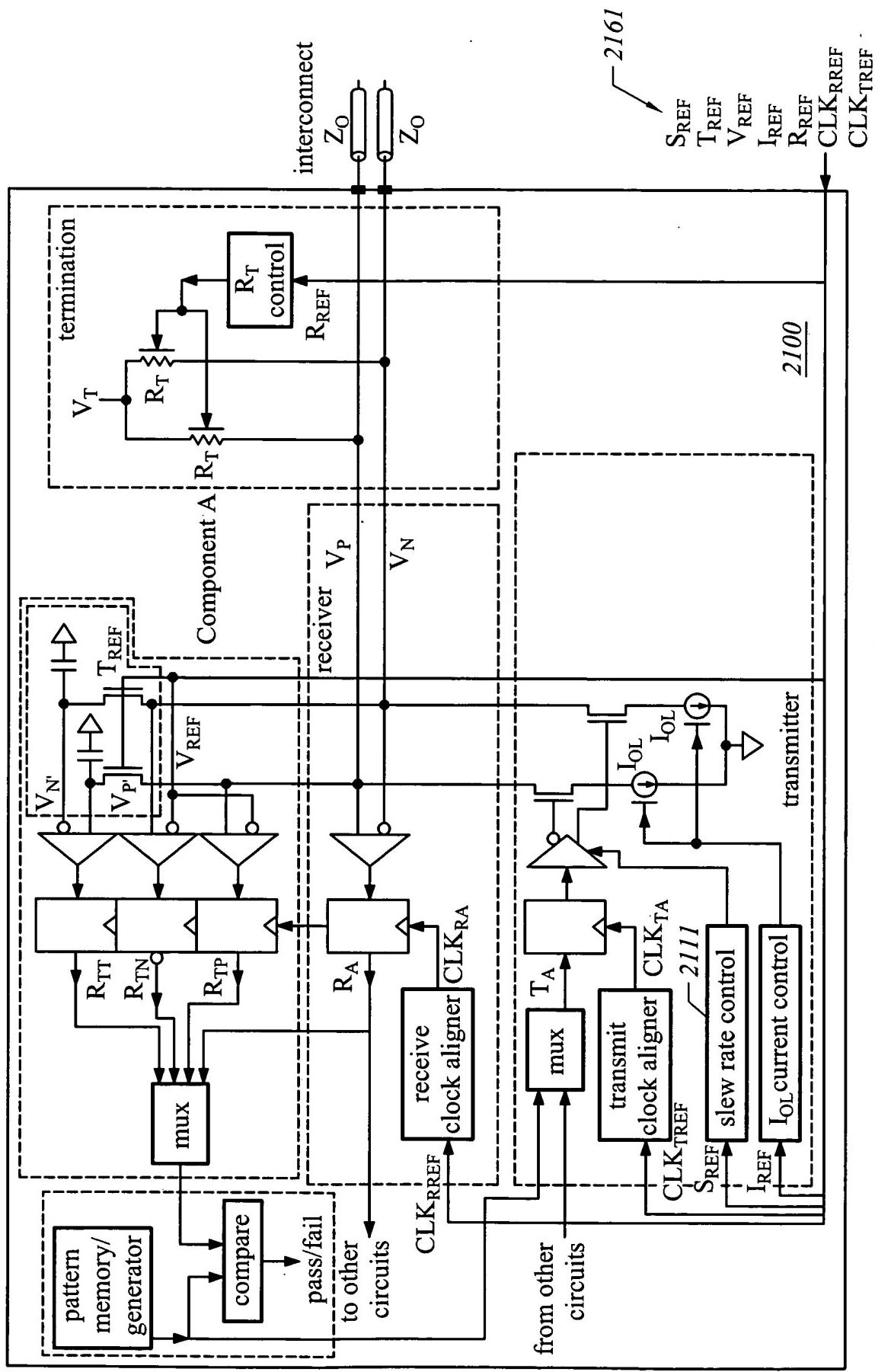


FIG. 21

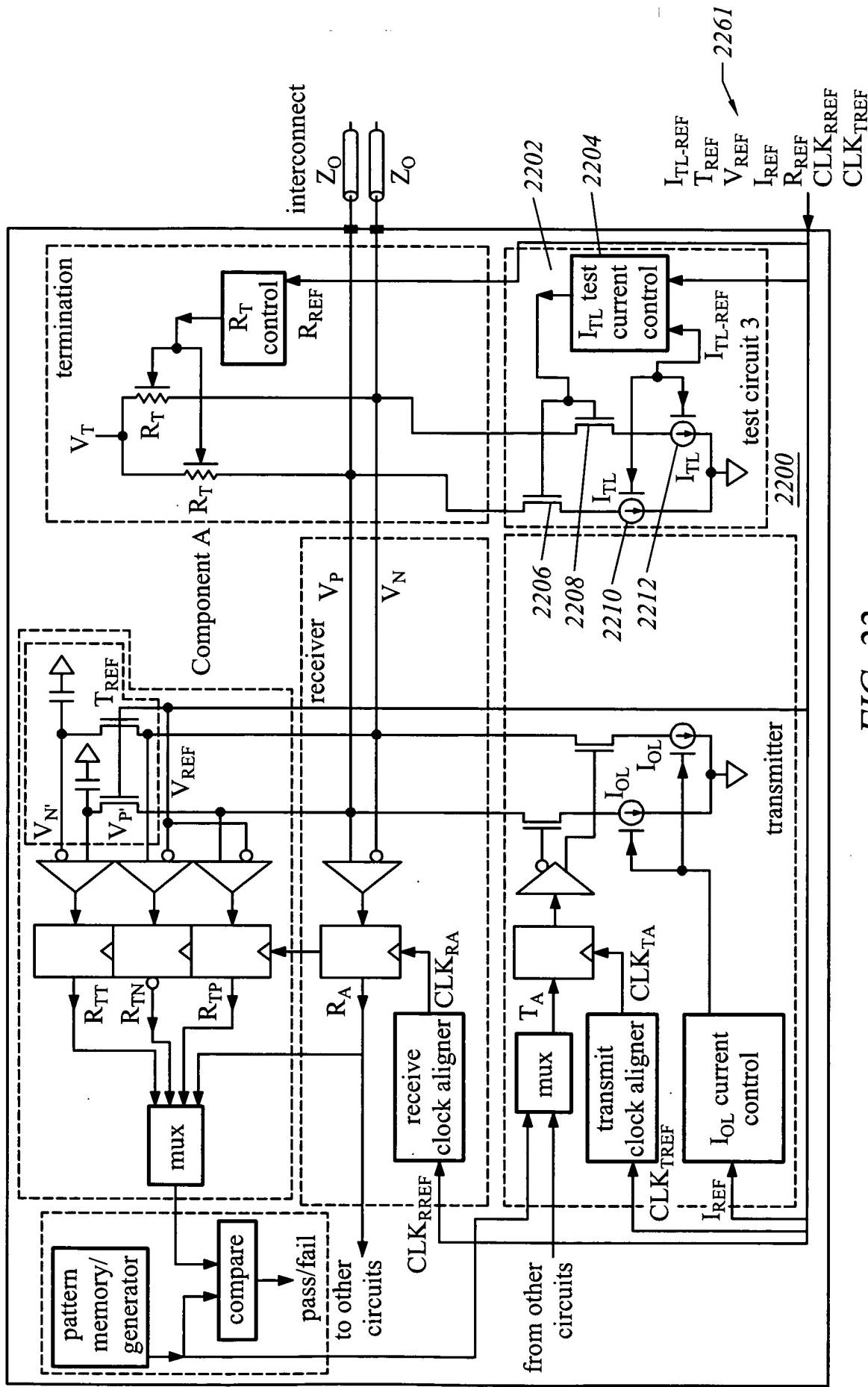
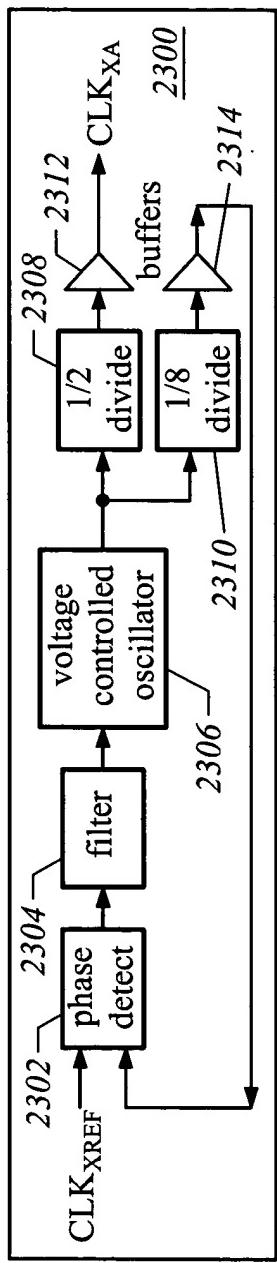


FIG. 22

FIG. 23A



Receive or transmit clock alignment using PLL with 4x frequency multiplication

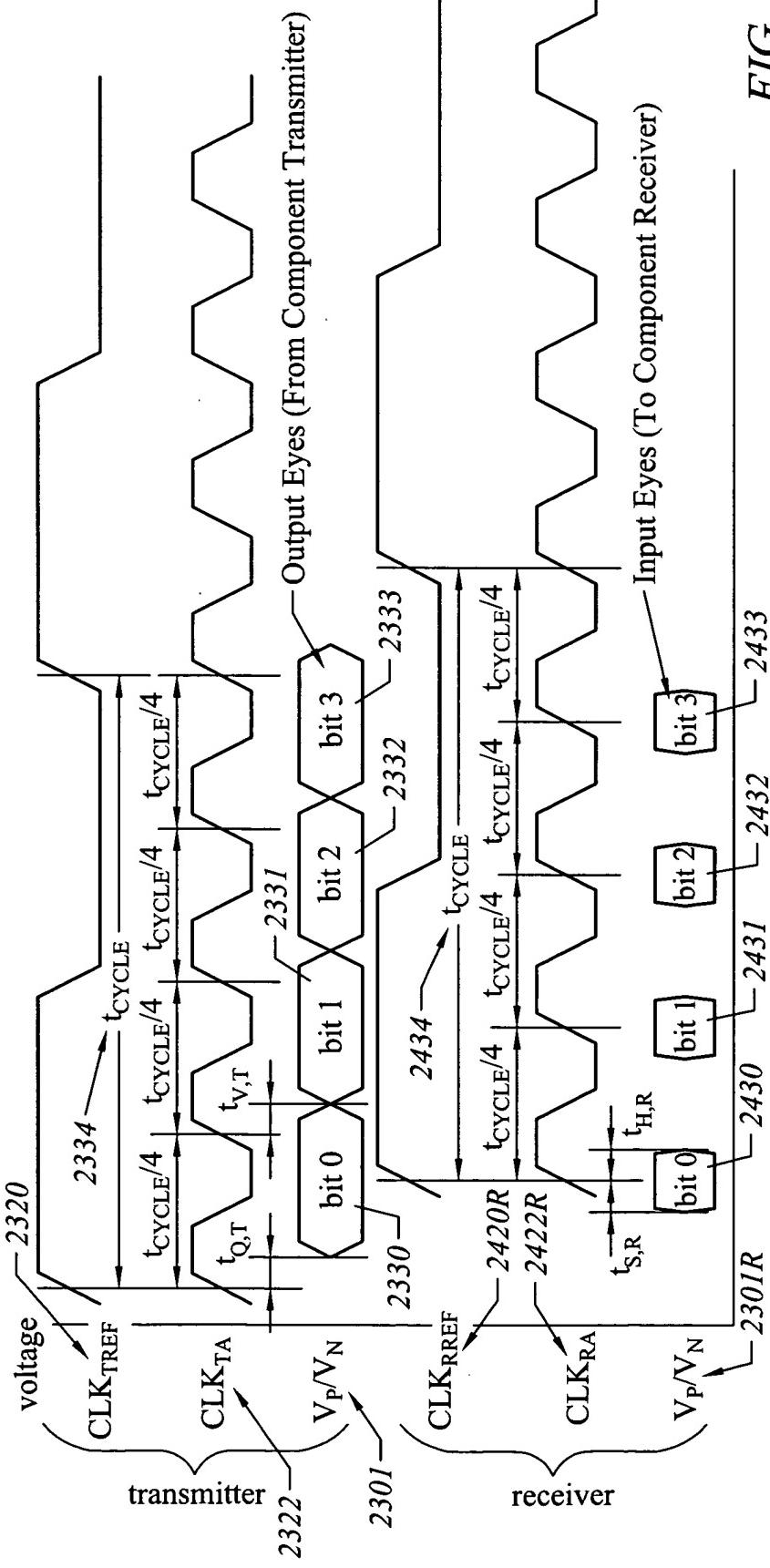


FIG. 23B

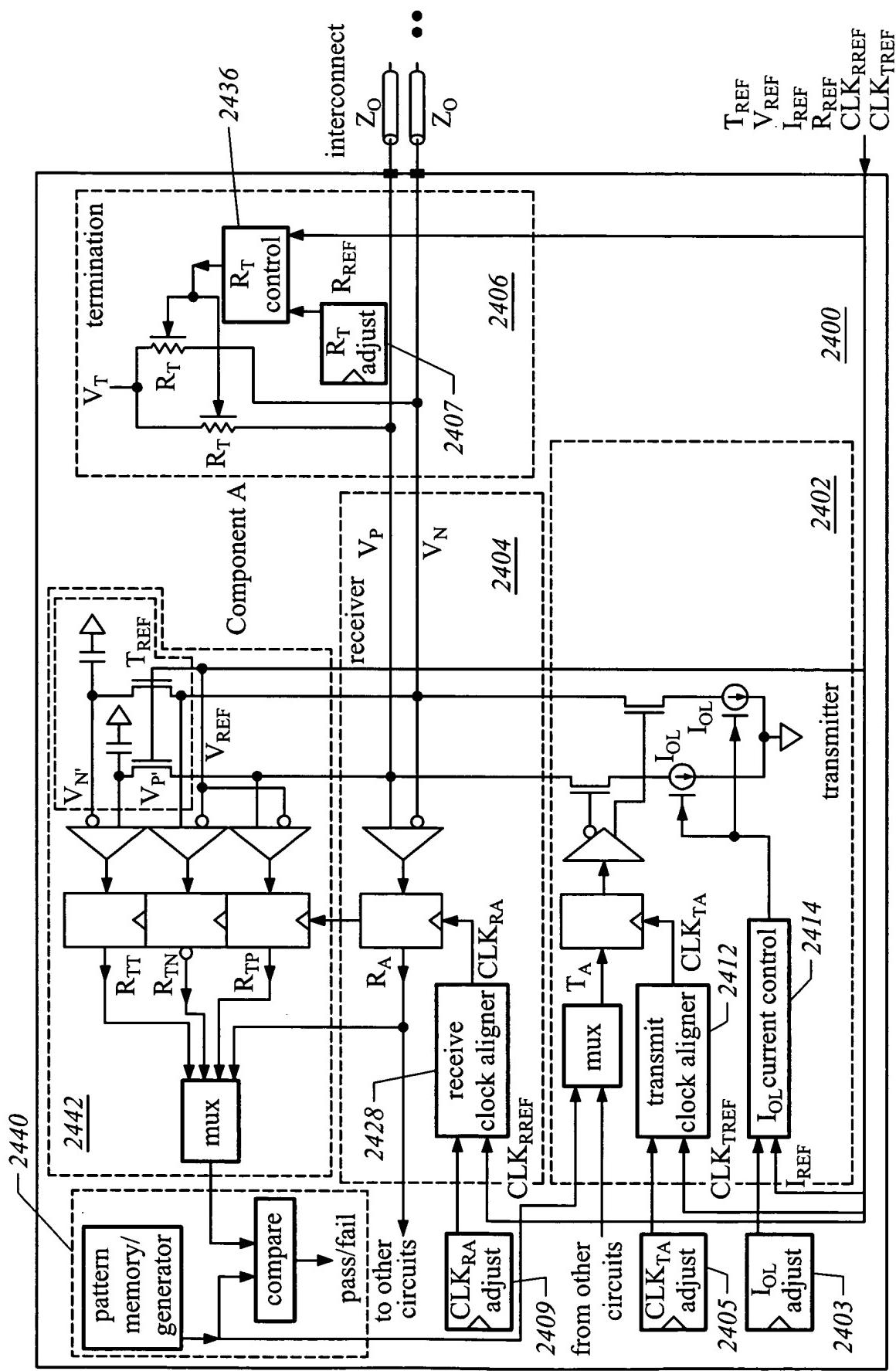


FIG. 24

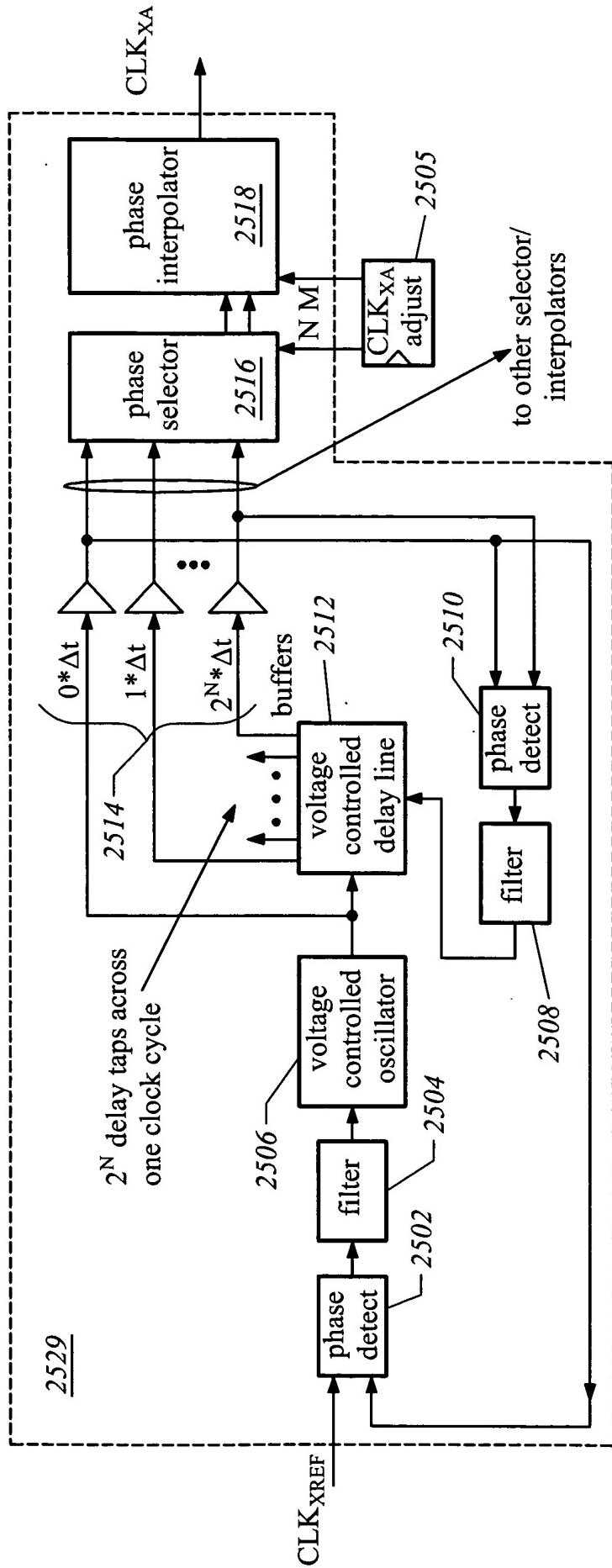
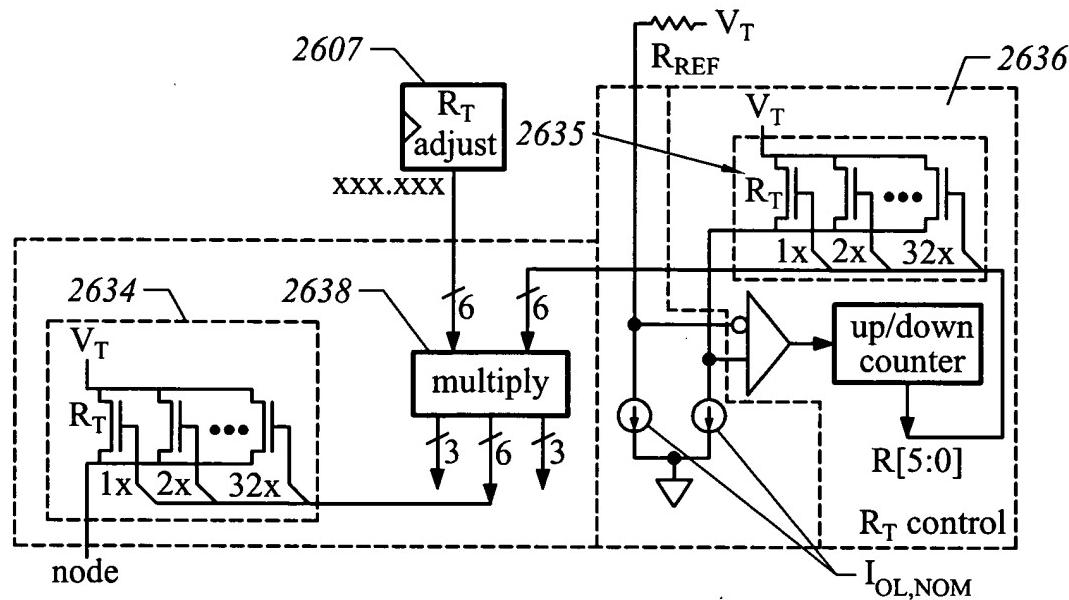
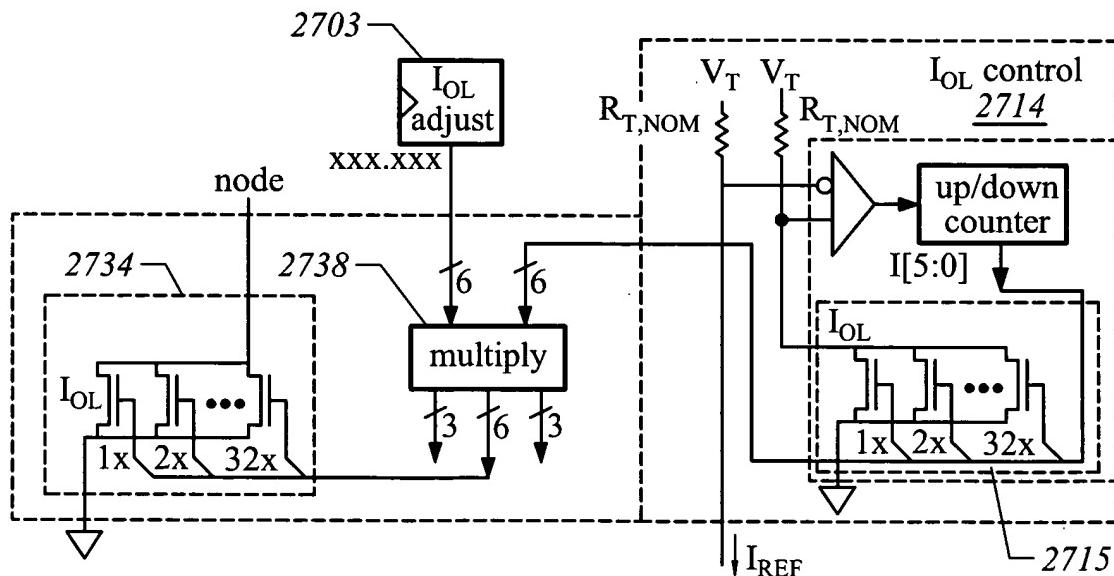


FIG. 25



Adjustable termination with calibration to reference value

FIG. 26



Adjustable I_{OL} current with calibration to reference value

FIG. 27

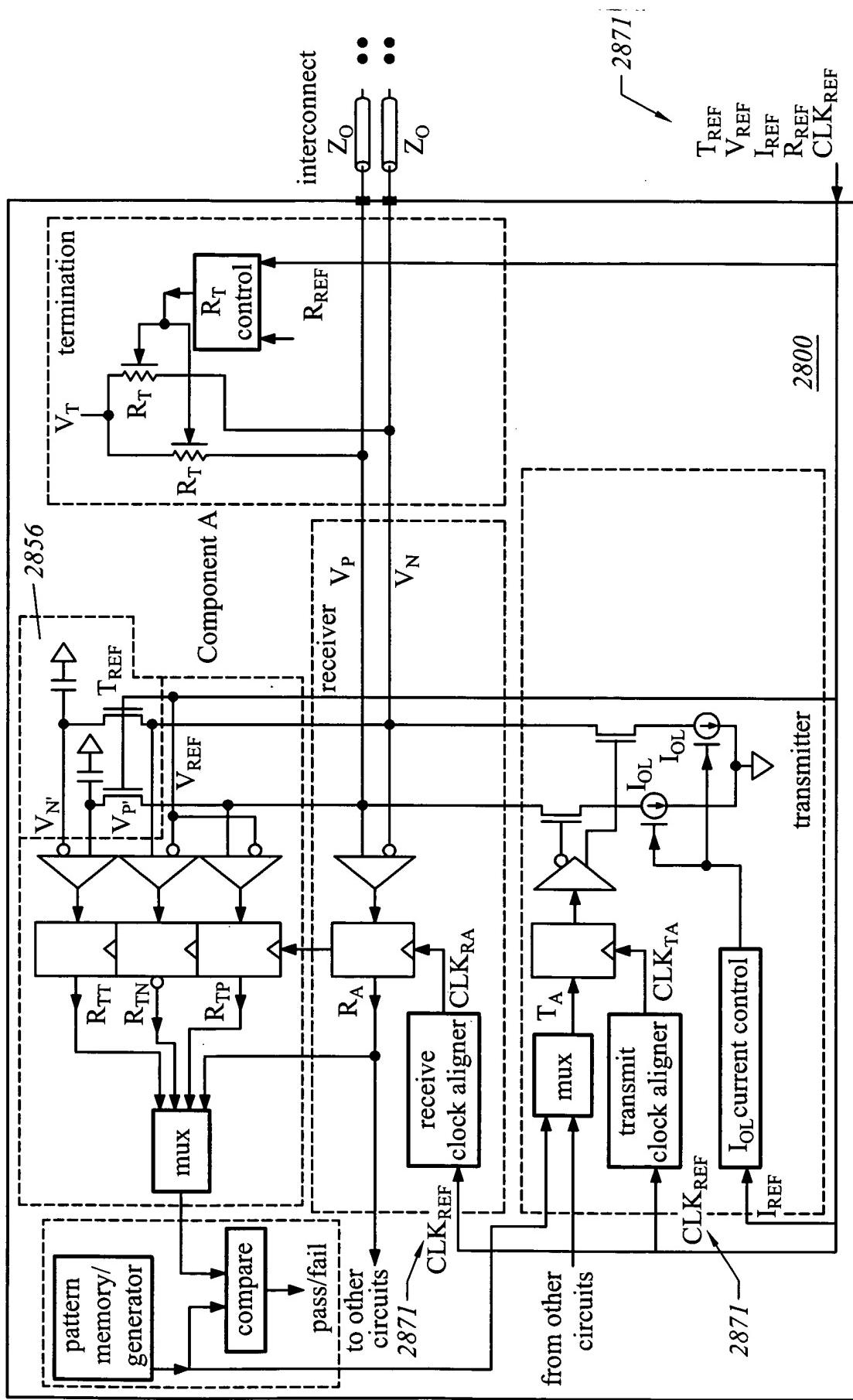


FIG. 28

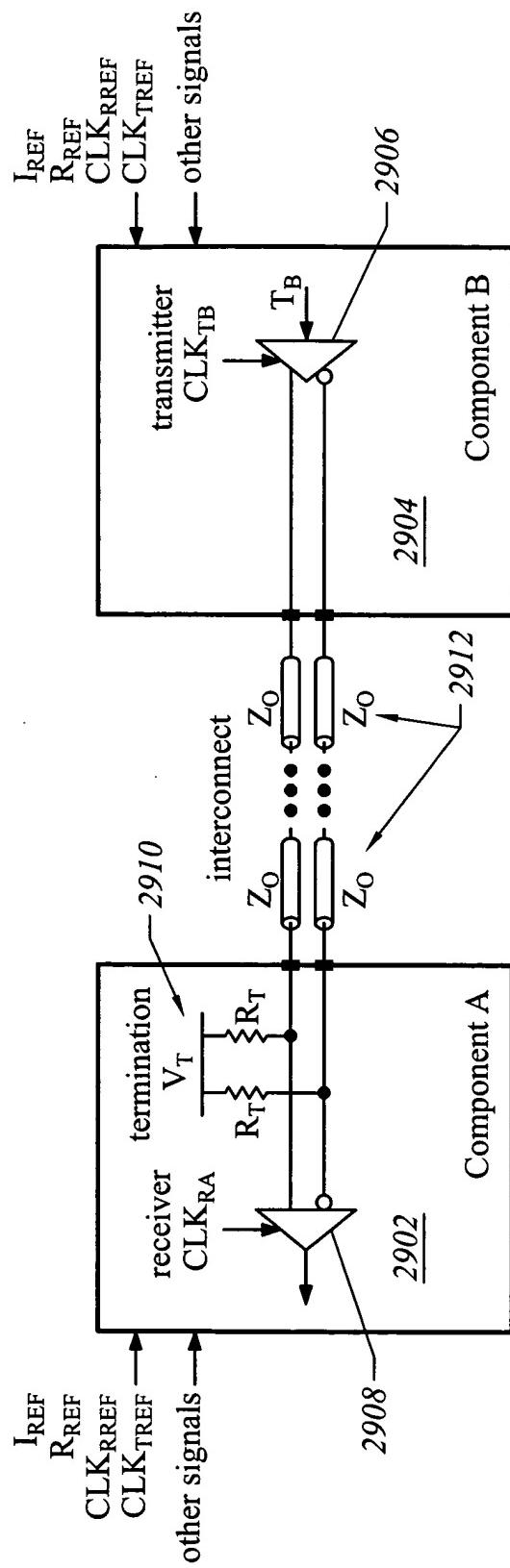


FIG. 29

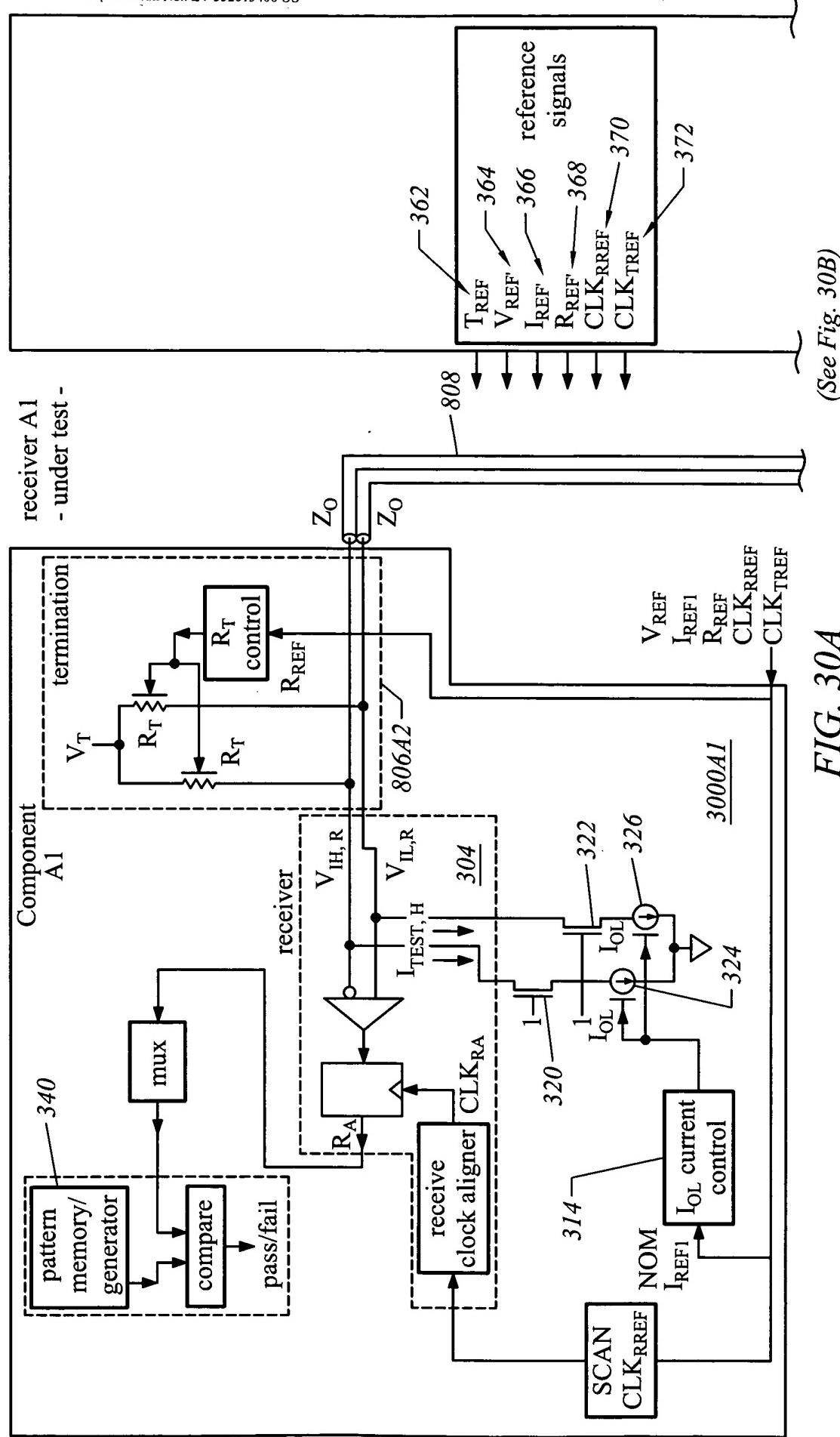


FIG. 30A

(See Fig. 30A)

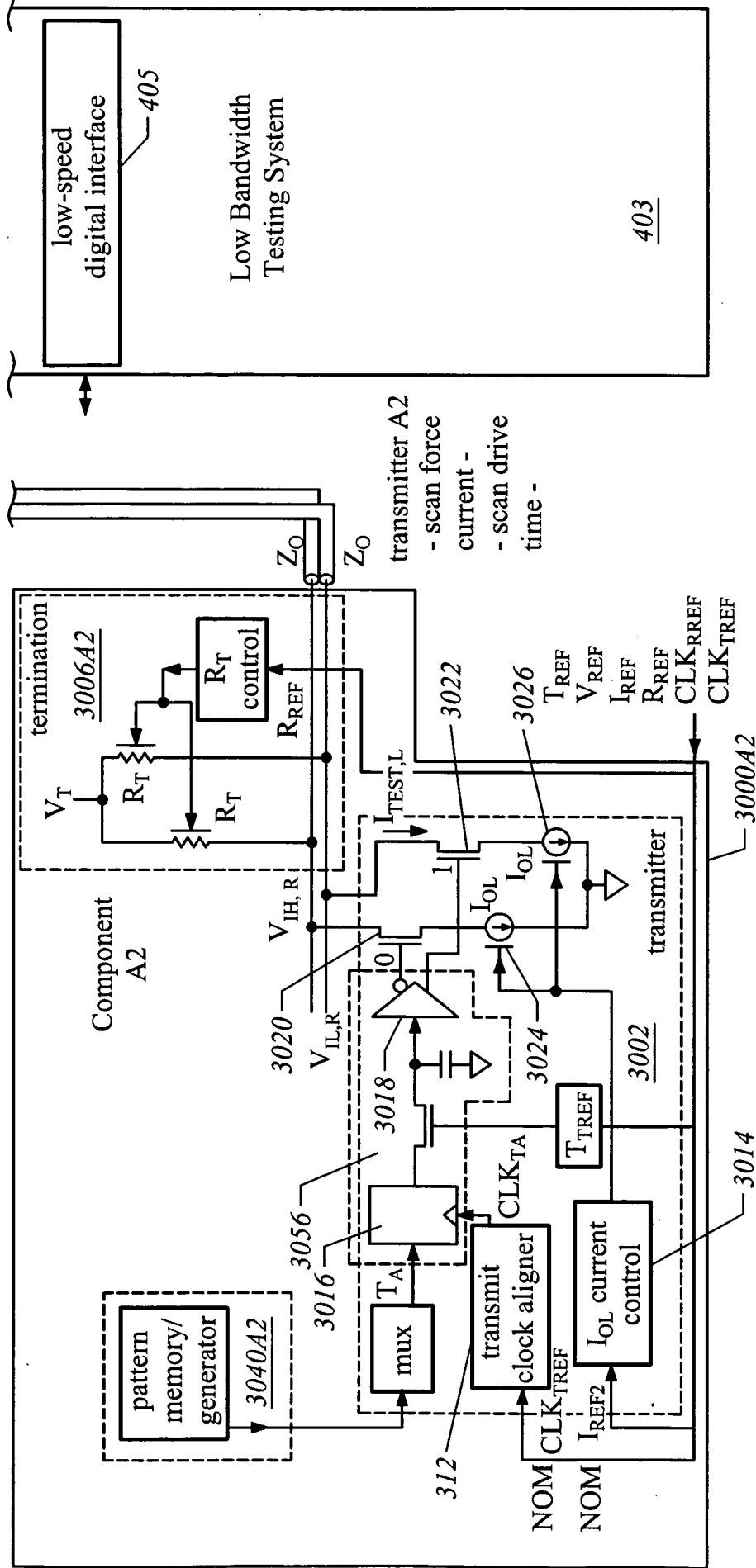


FIG. 30B

Title: Method And Apparatus For Test And Characterization Of Semiconductor Components
 Applicants: Ware et al. Docket: RAMB-01033US1
 Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
 Filing Date: January 30, 2004 Phone: (415) 369-9660
 Express Mail No.: EV 332013406 US

transmitter t_Q/t_V receiver $t_S + t_Q = k1$ $t_V - t_H = k2$ transmitter => receiver

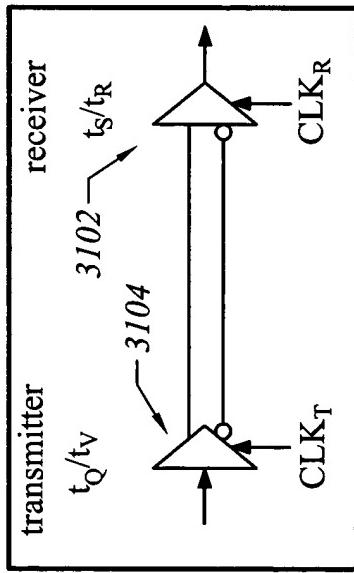


FIG. 31

3202 transmitter t_Q/t_V receiver $t_S + t_Q = k1$ $t_V - t_H = k2$ transmitter => receiver
 sampler 1 t_{S1}/t_{R1} t_{Q1}/t_{V1} $t_{S1} + t_Q = k3$ $t_V - t_{H1} = k4$ transmitter => sampler 1
 $t_{S1} + t_{Q1} = k7$ $t_{V1} - t_H = k8$ sampler 1 => receiver

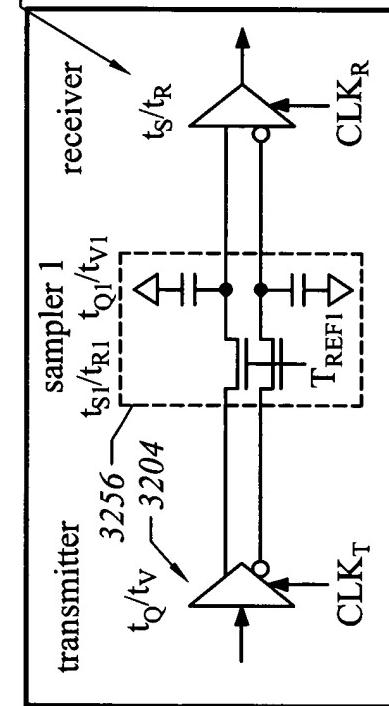
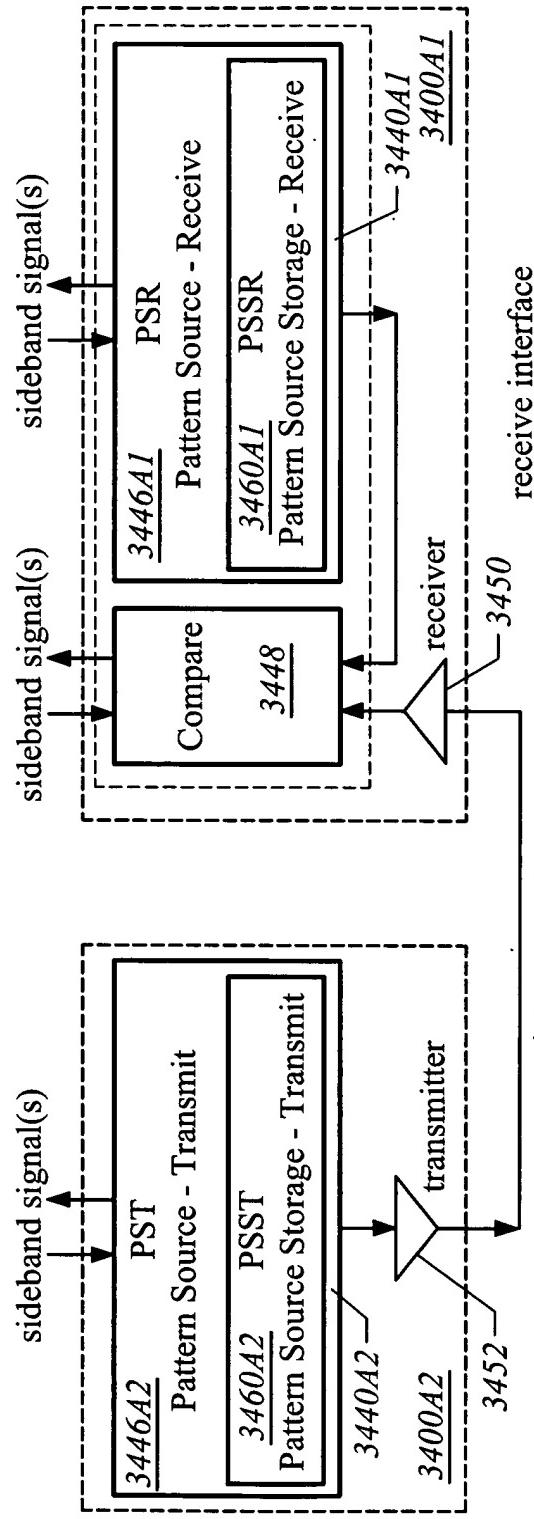
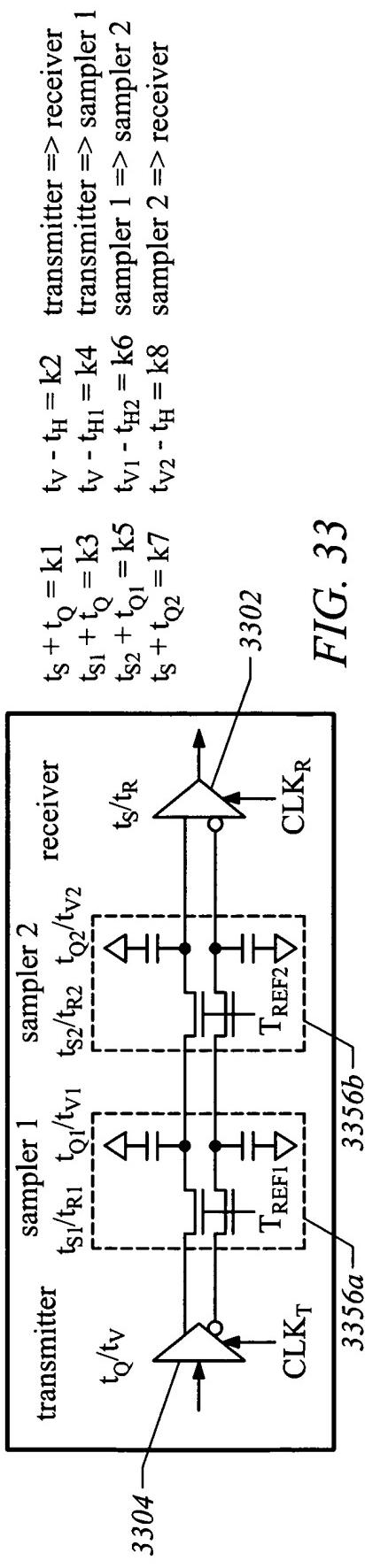


FIG. 32



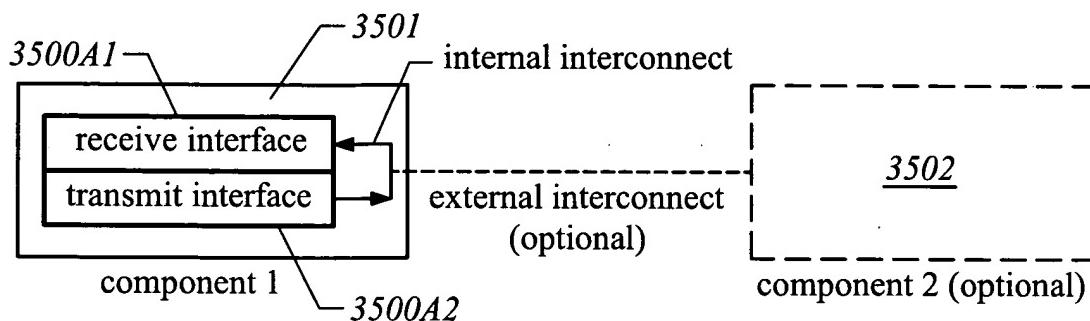


FIG. 35A

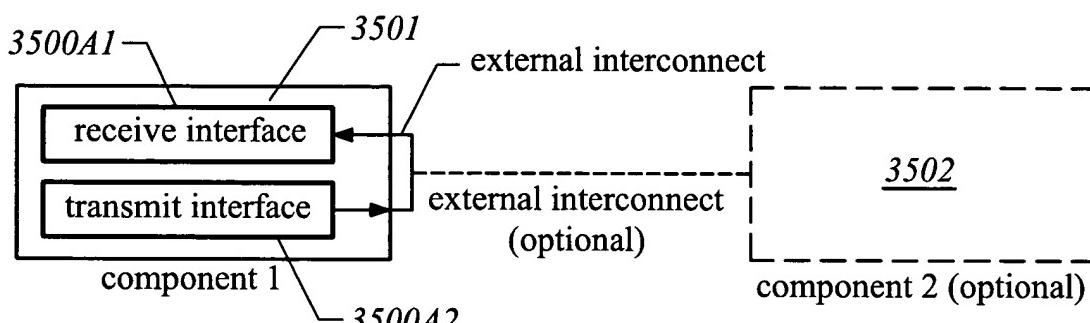


FIG. 35B

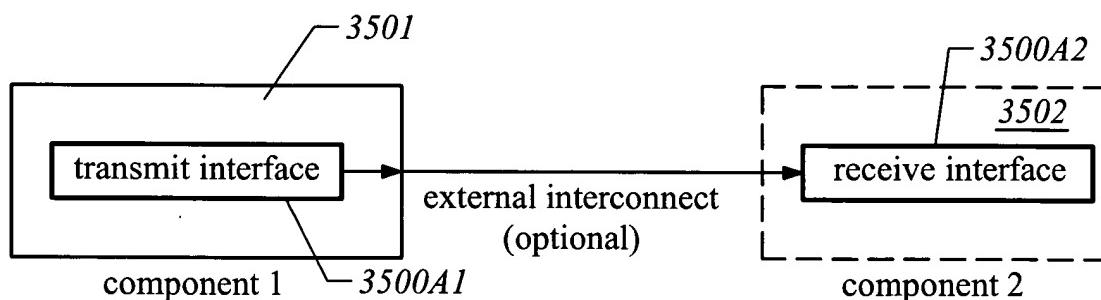


FIG. 35C

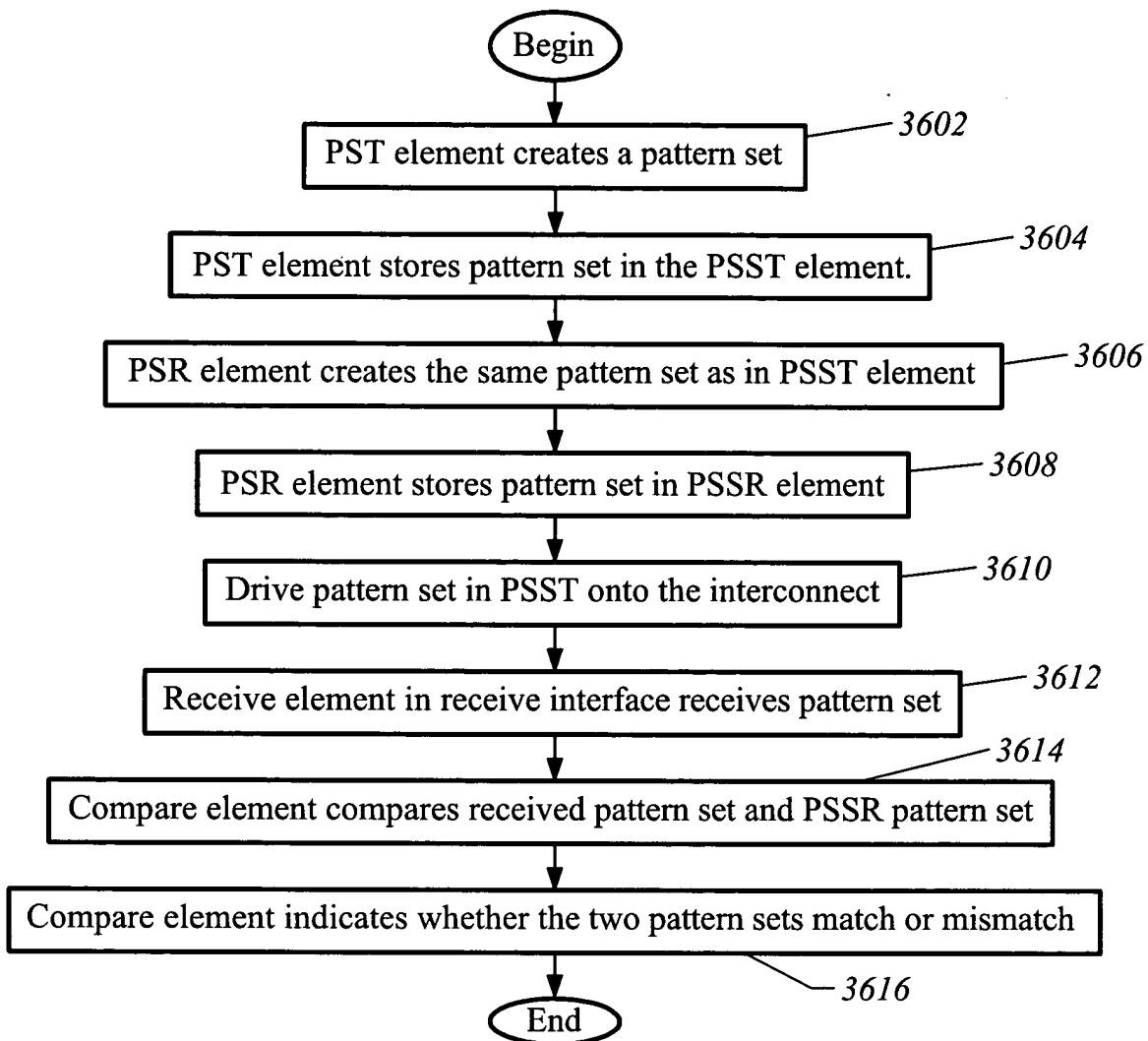


FIG. 36

Title: Method And Apparatus For Test And Characterization Of Semiconductor Components
 Applicants: Ware et al. Docket: RAMB-01033US1
 Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
 Filing Date: January 30, 2004 Phone: (415) 369-9660
 Express Mail No.: EV 332013406 US

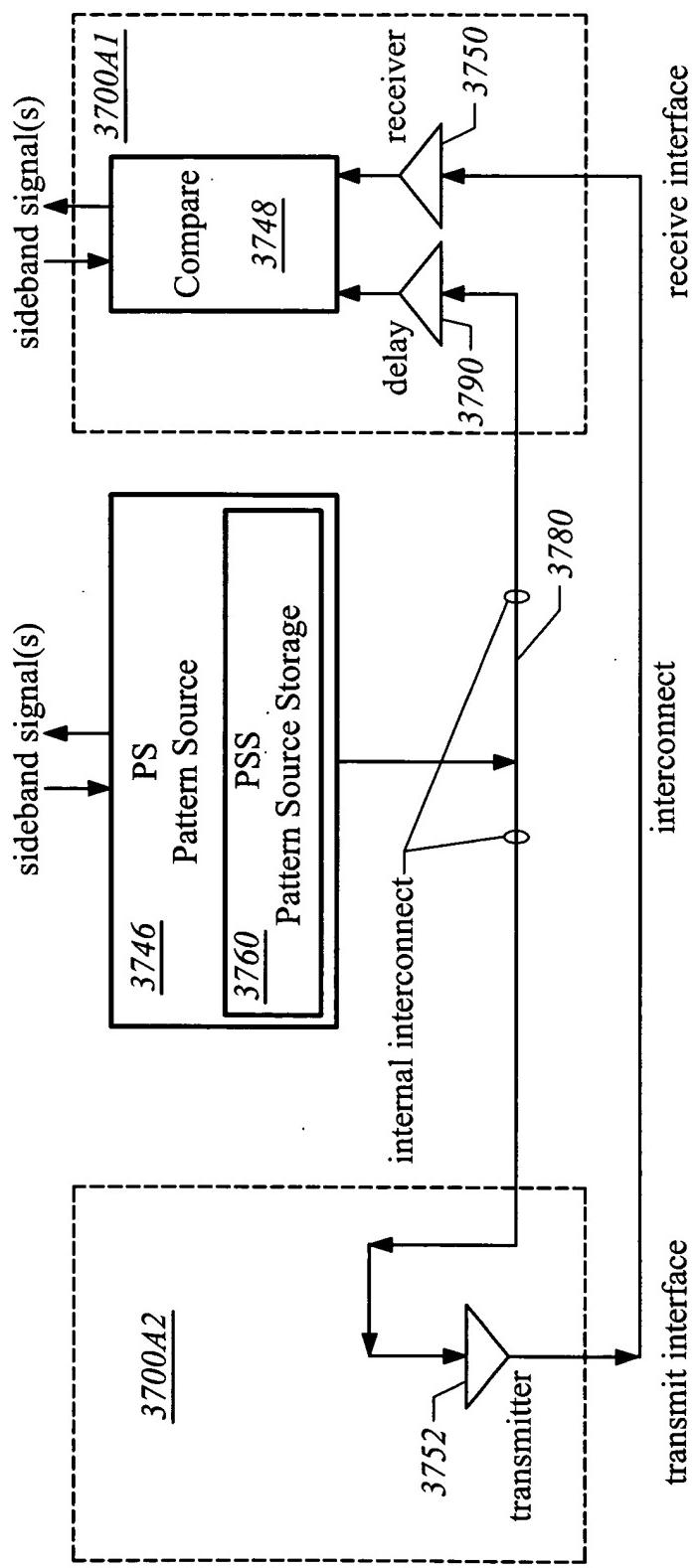


FIG. 37

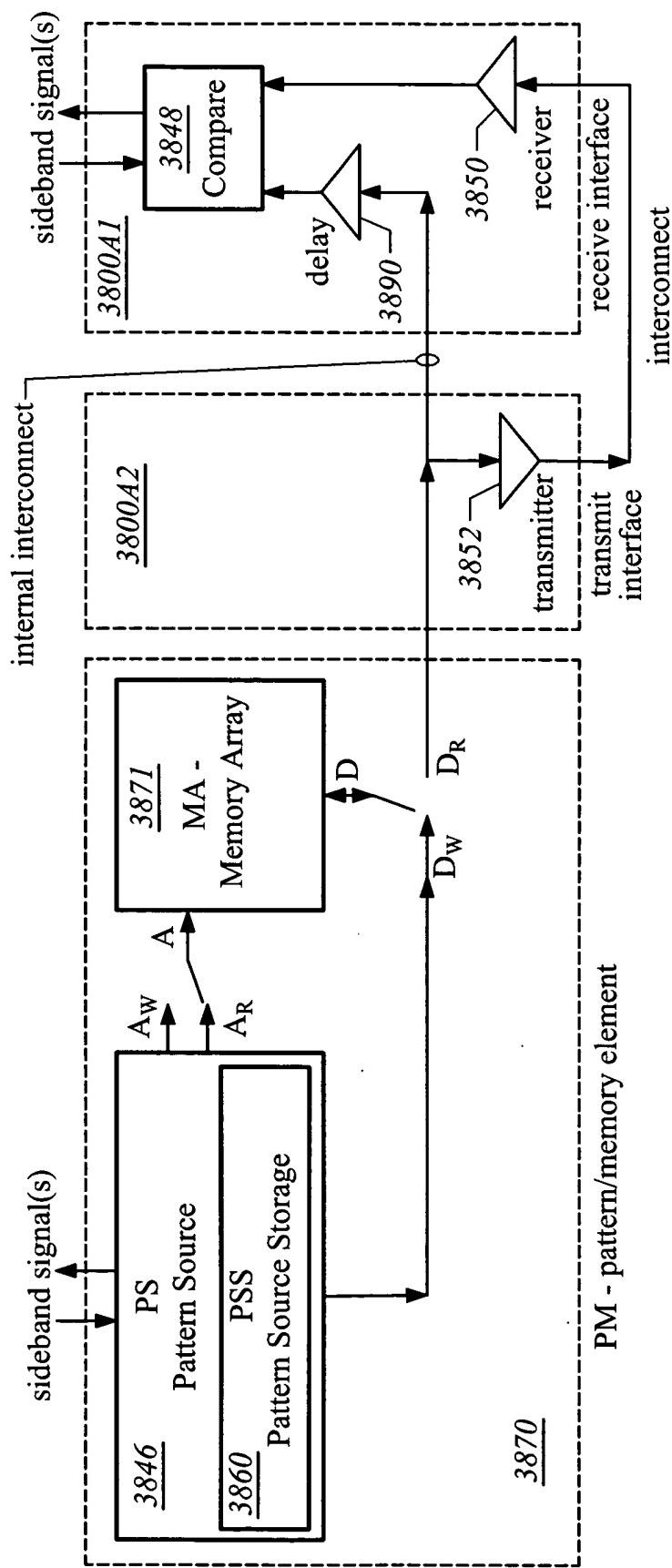


FIG. 38

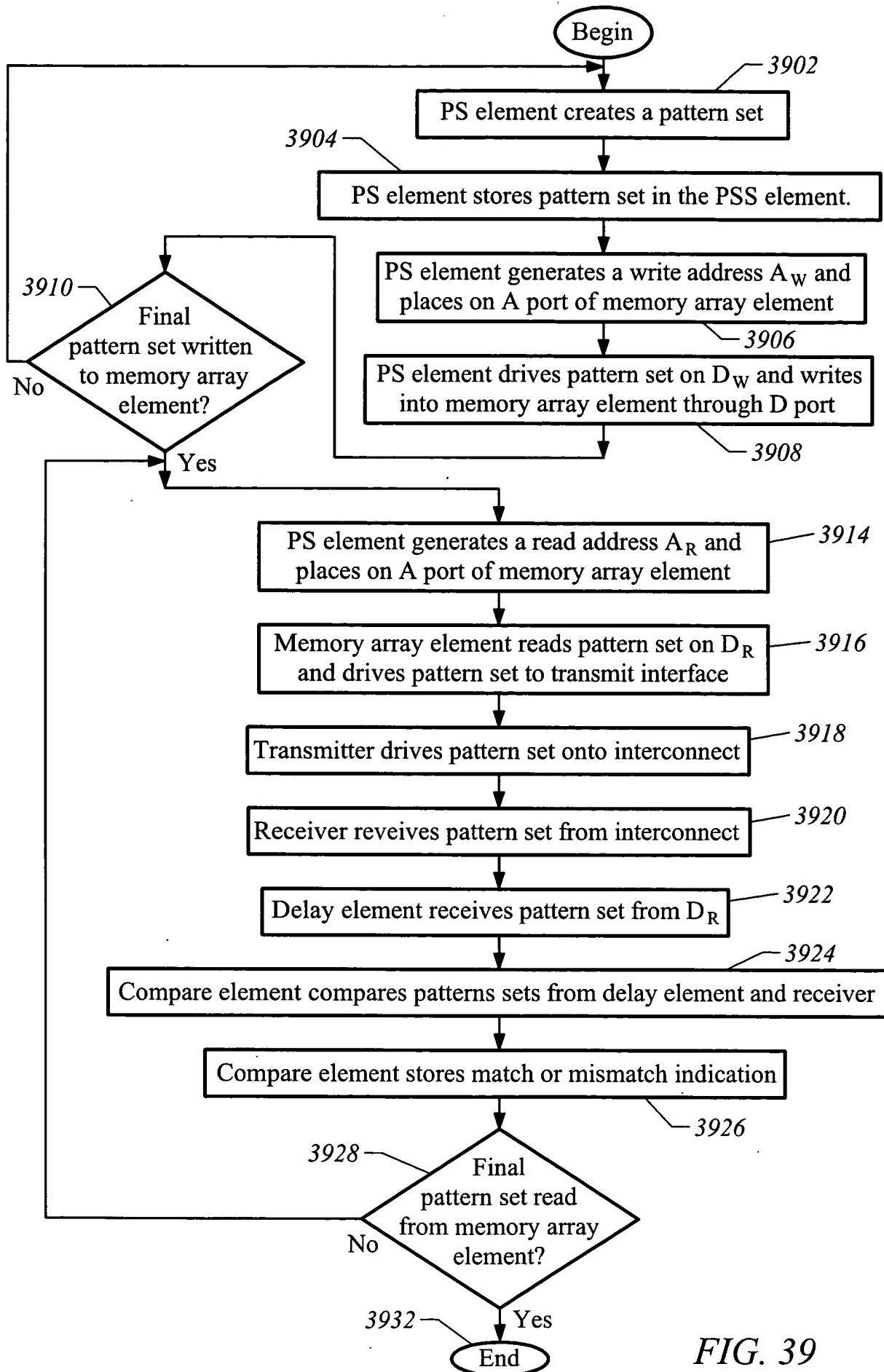
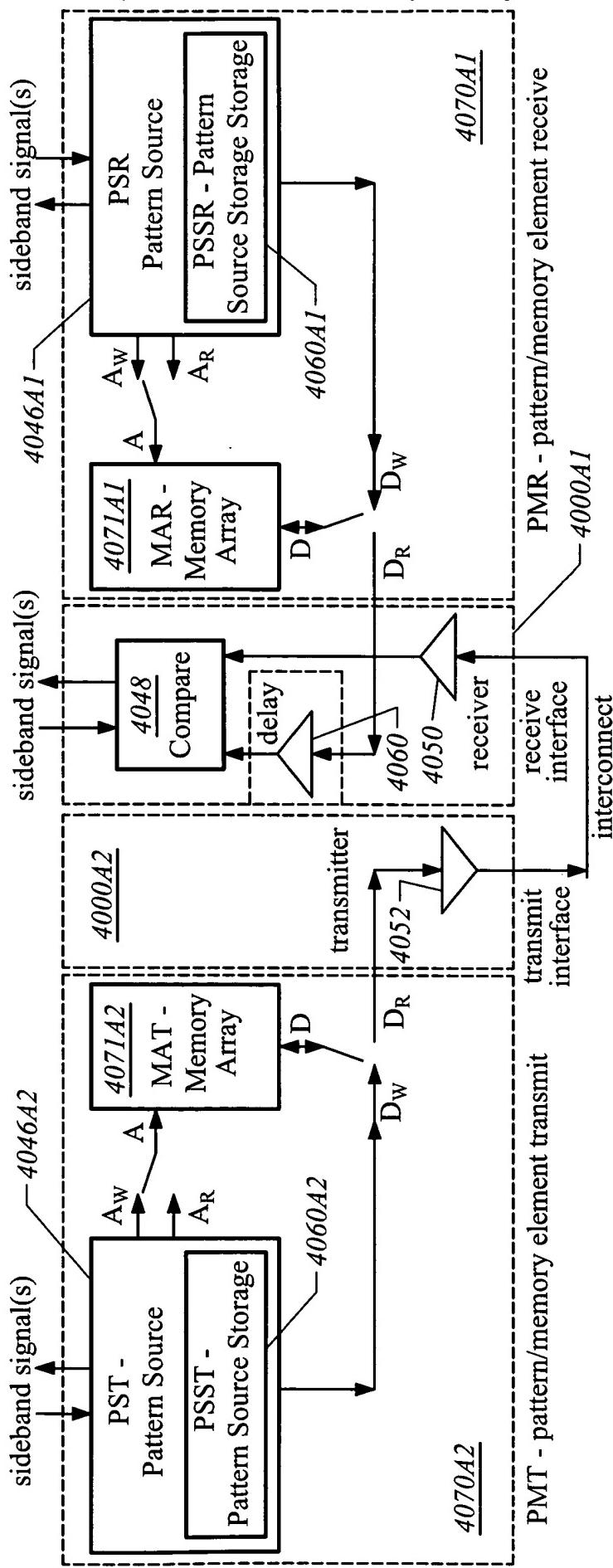
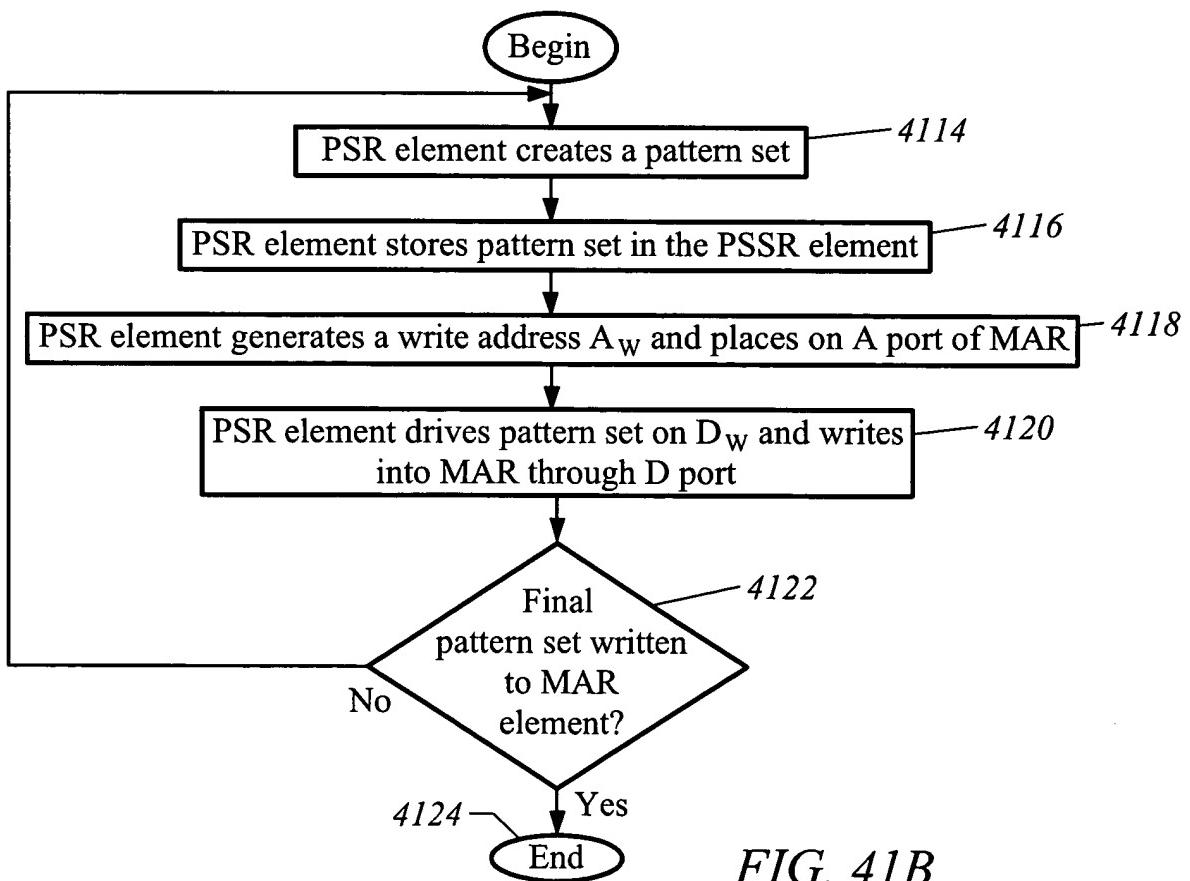
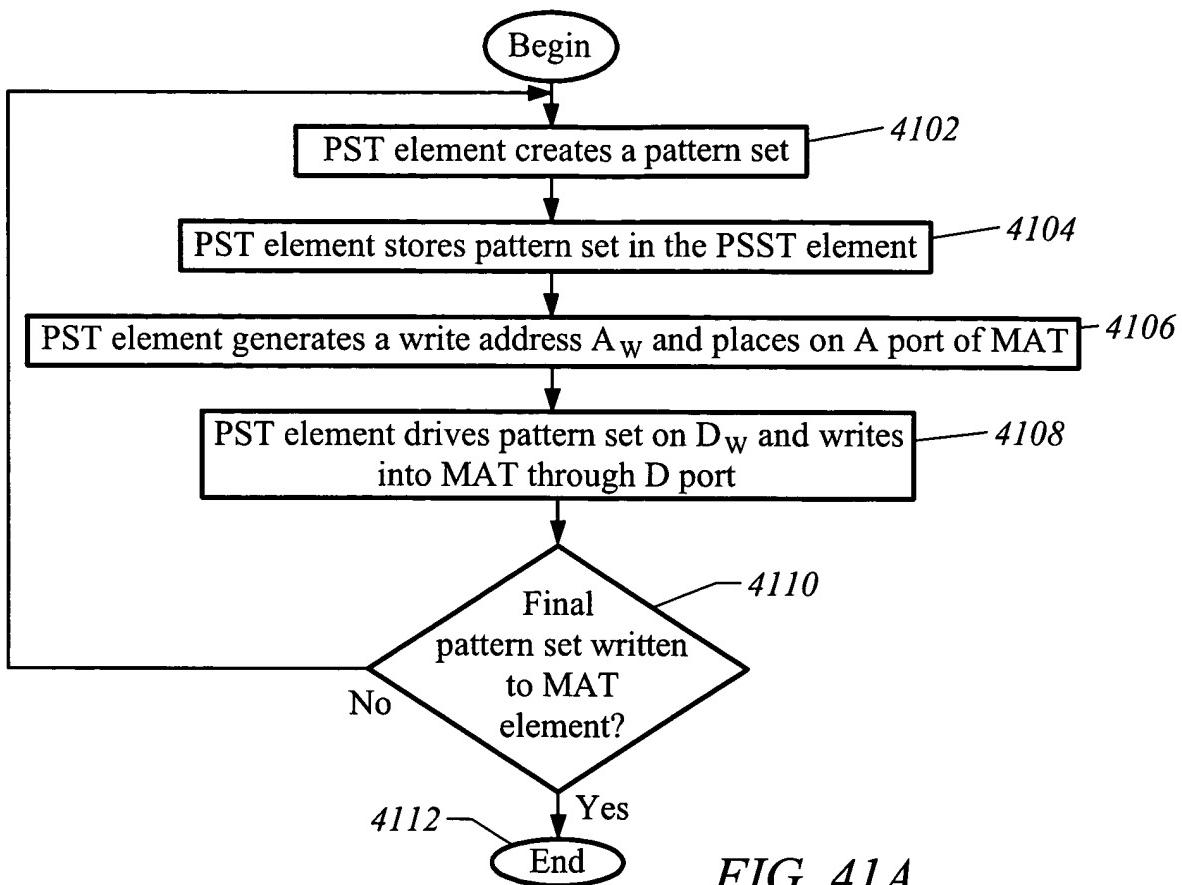


FIG. 39





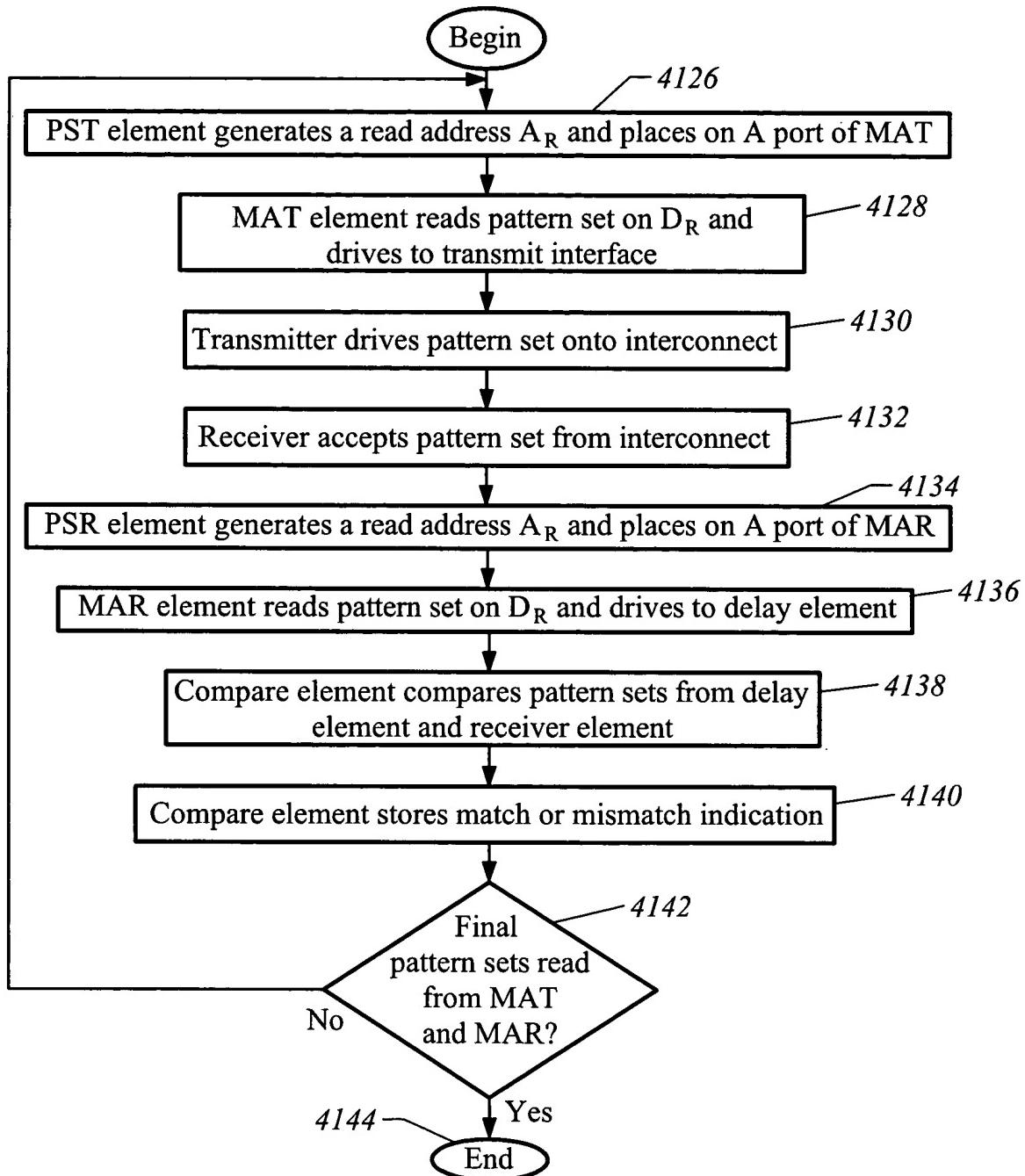


FIG. 41C

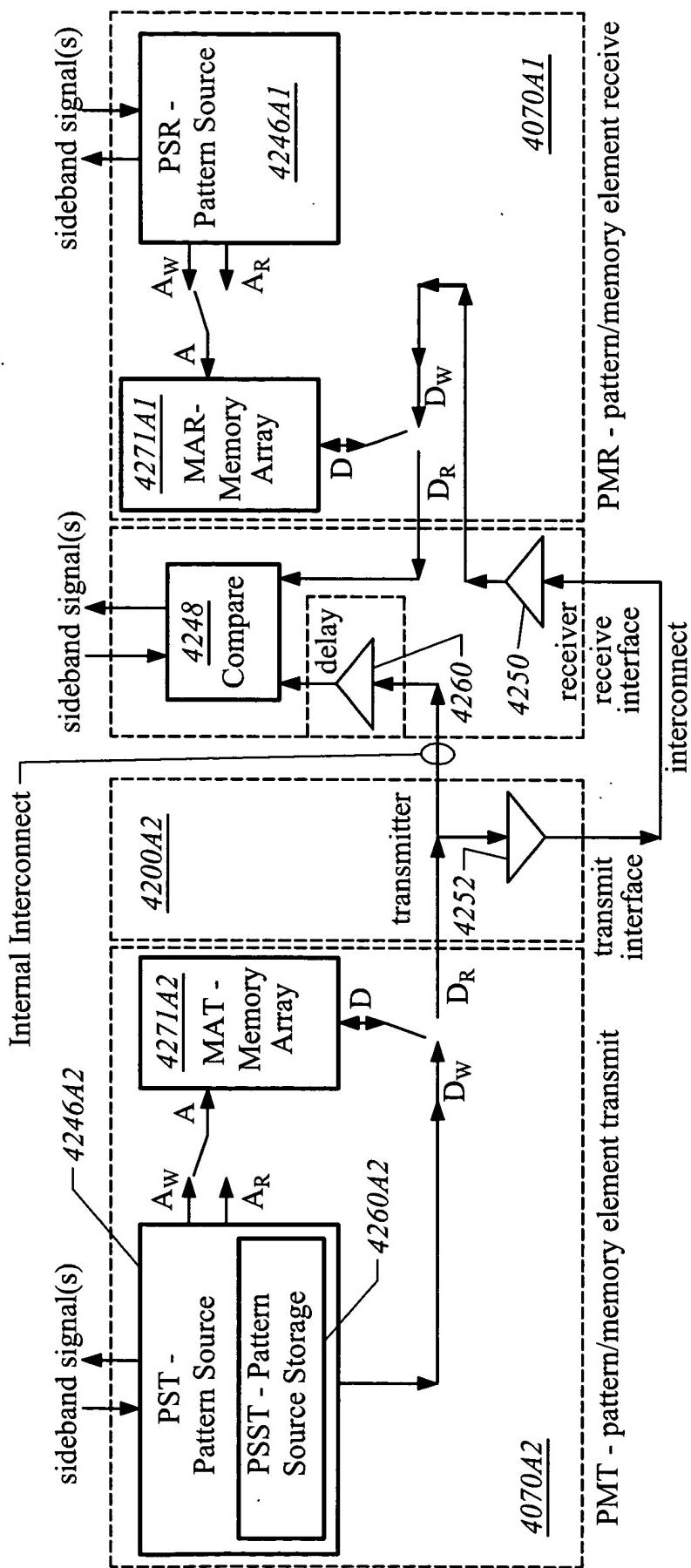


FIG. 42

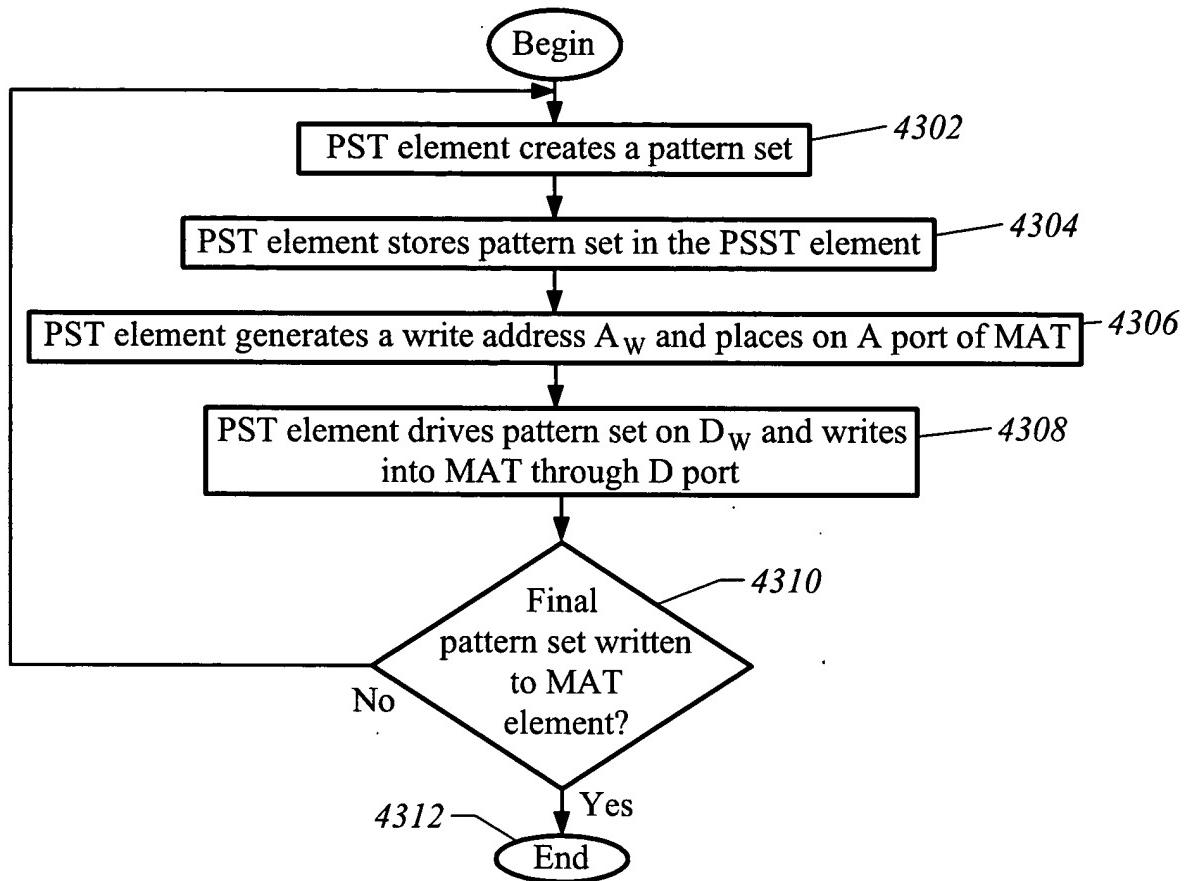


FIG. 43A

Title: Method And Apparatus For Test And Characterization Of Semiconductor Components
 Applicants: Ware et al. Docket: RAMB-01033US1
 Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
 Filing Date: January 30, 2004 Phone: (415) 369-9660
 Express Mail No.: EV 332013406 US

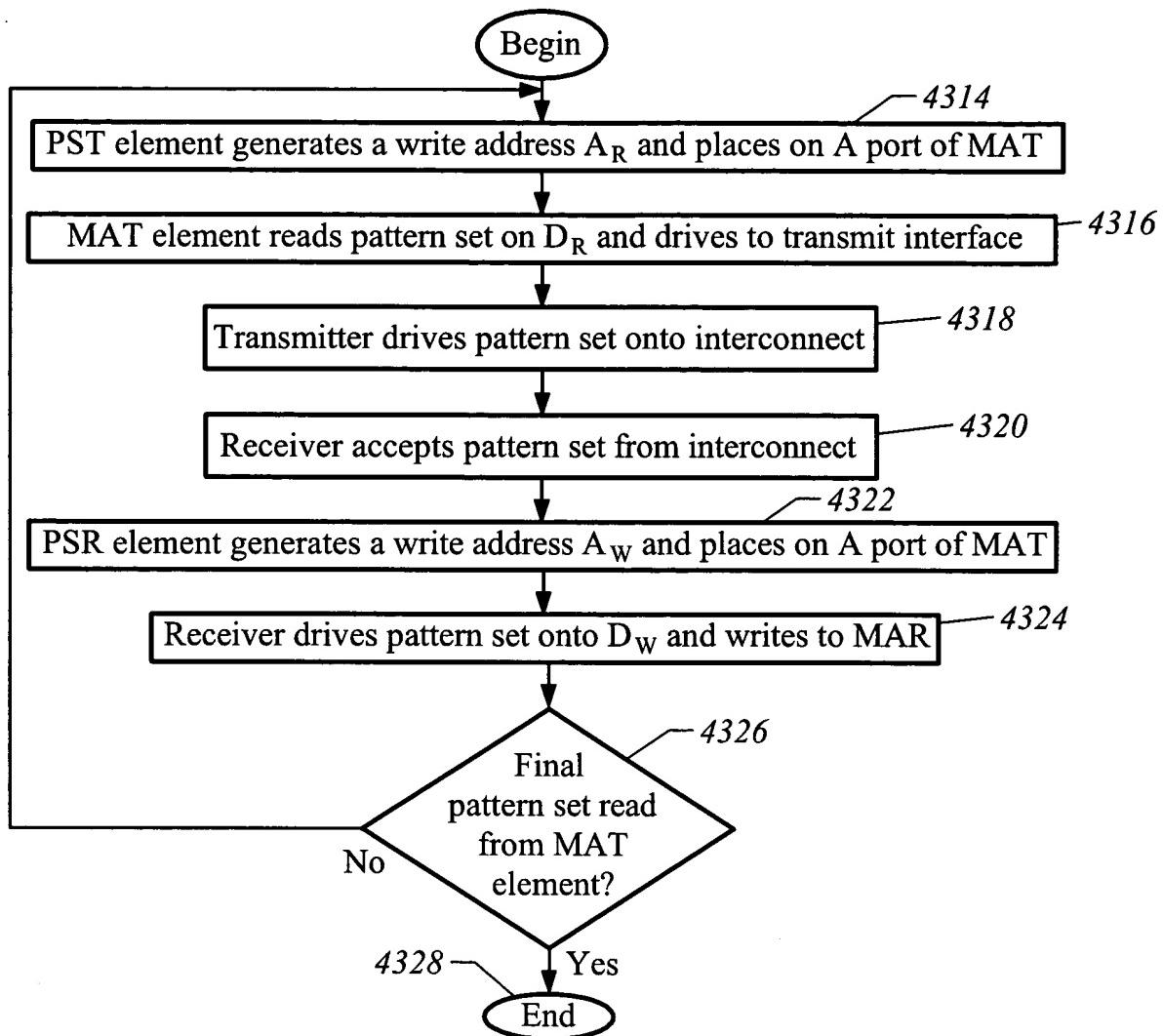


FIG. 43B

Title: Method And Apparatus For Test And Characterization Of Semiconductor Components
 Applicants: Ware et al. Docket: RAMB-01033US1
 Appl. No.: Unknown Atty: Kirk J. DeNiro, Esq.
 Filing Date: January 30, 2004 Phone: (415) 369-9660
 Express Mail No.: EV 332013406 US

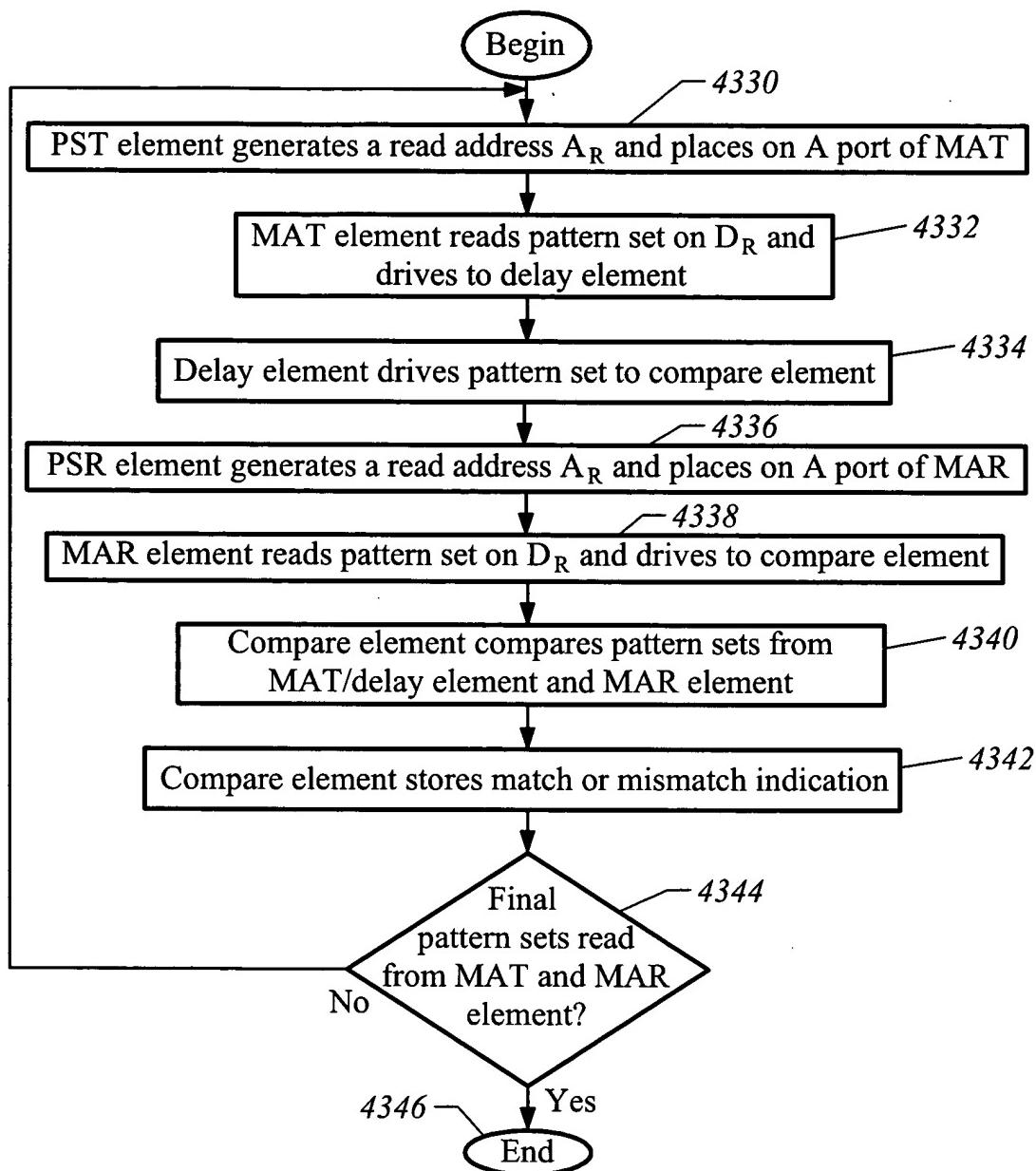
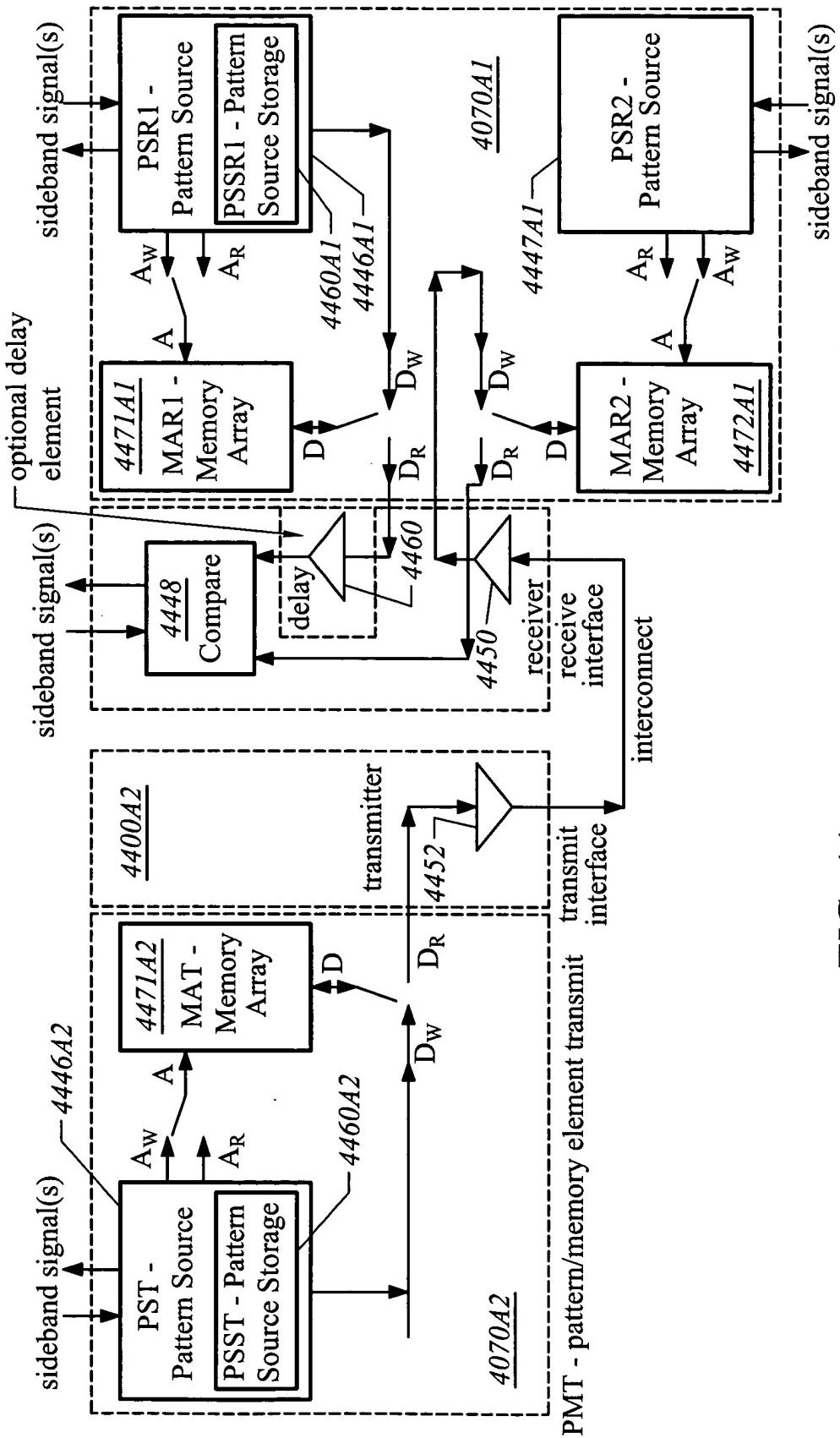


FIG. 43C



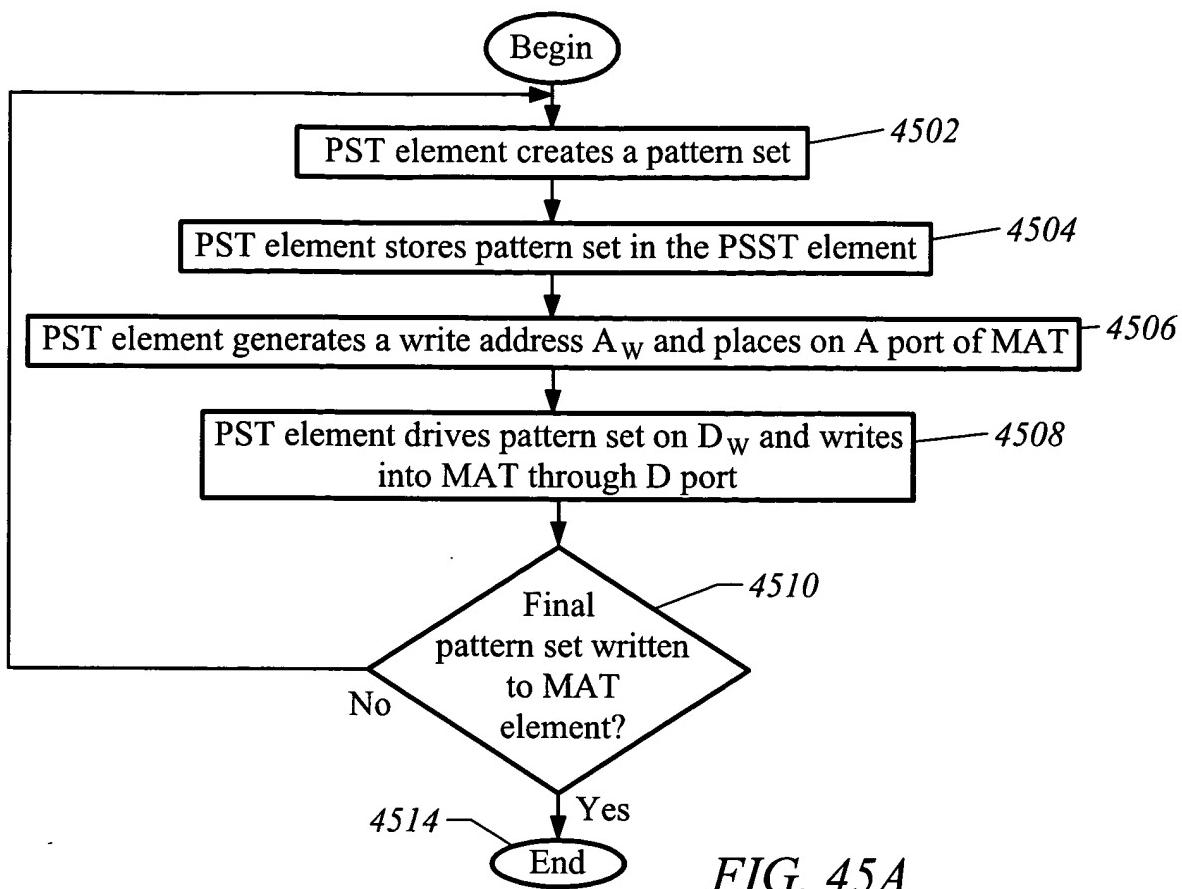


FIG. 45A

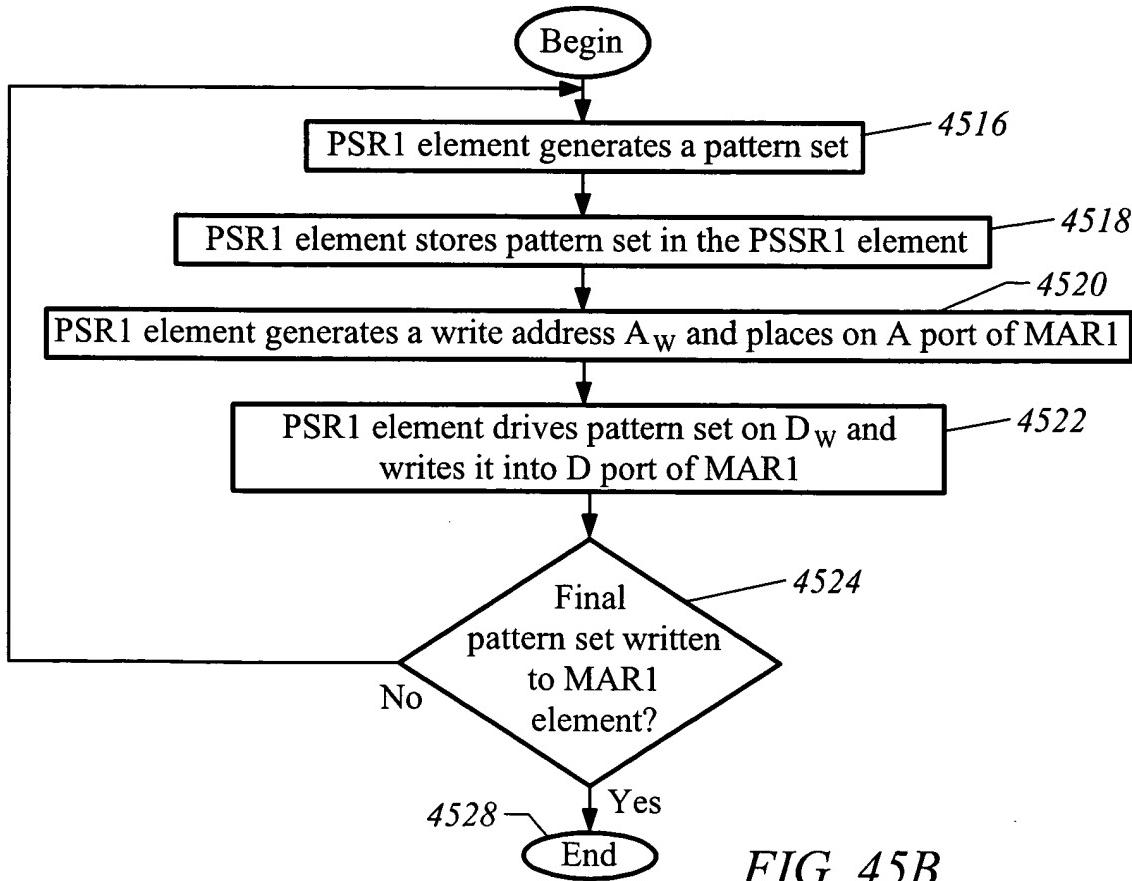


FIG. 45B

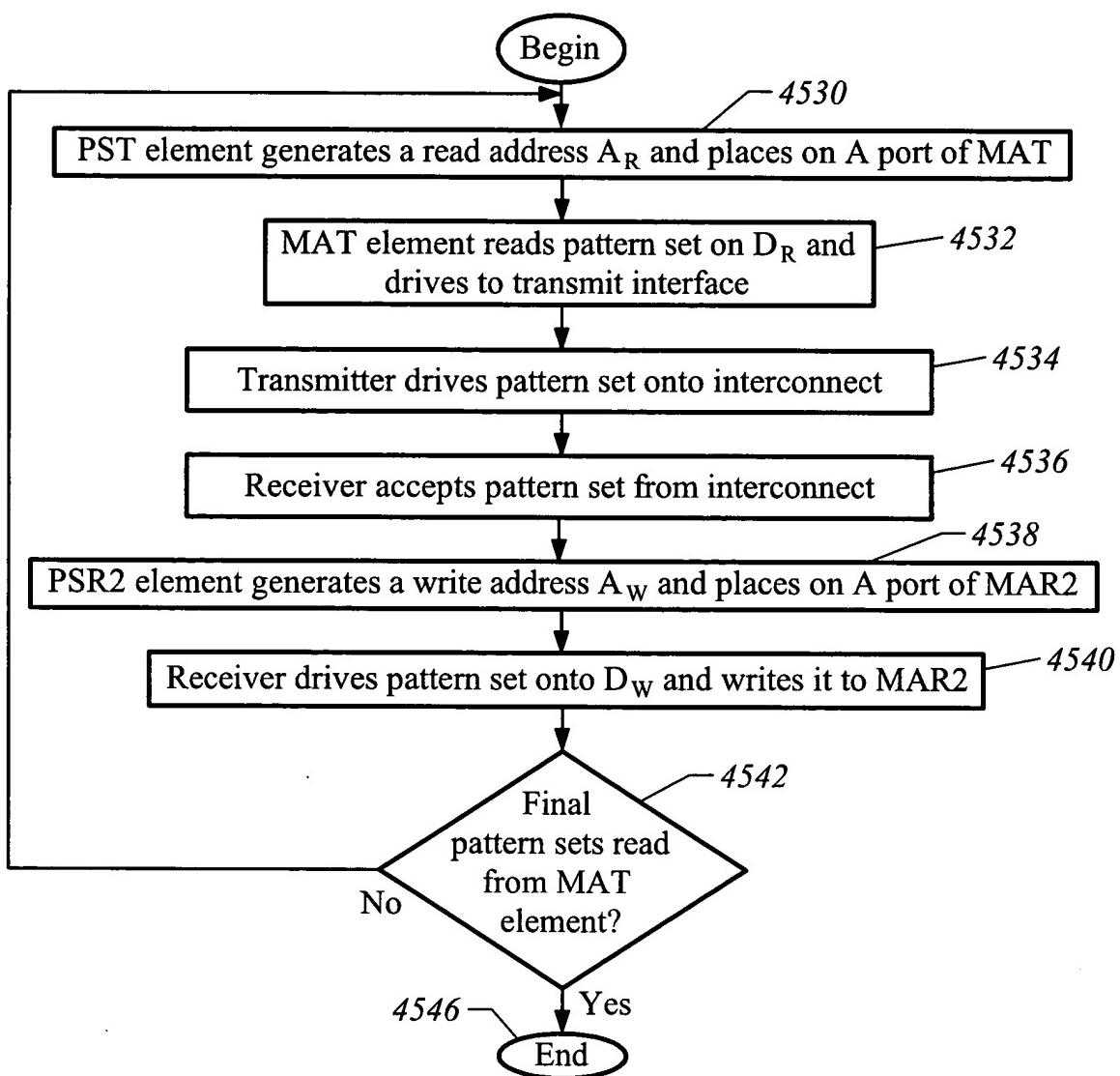


FIG. 45C

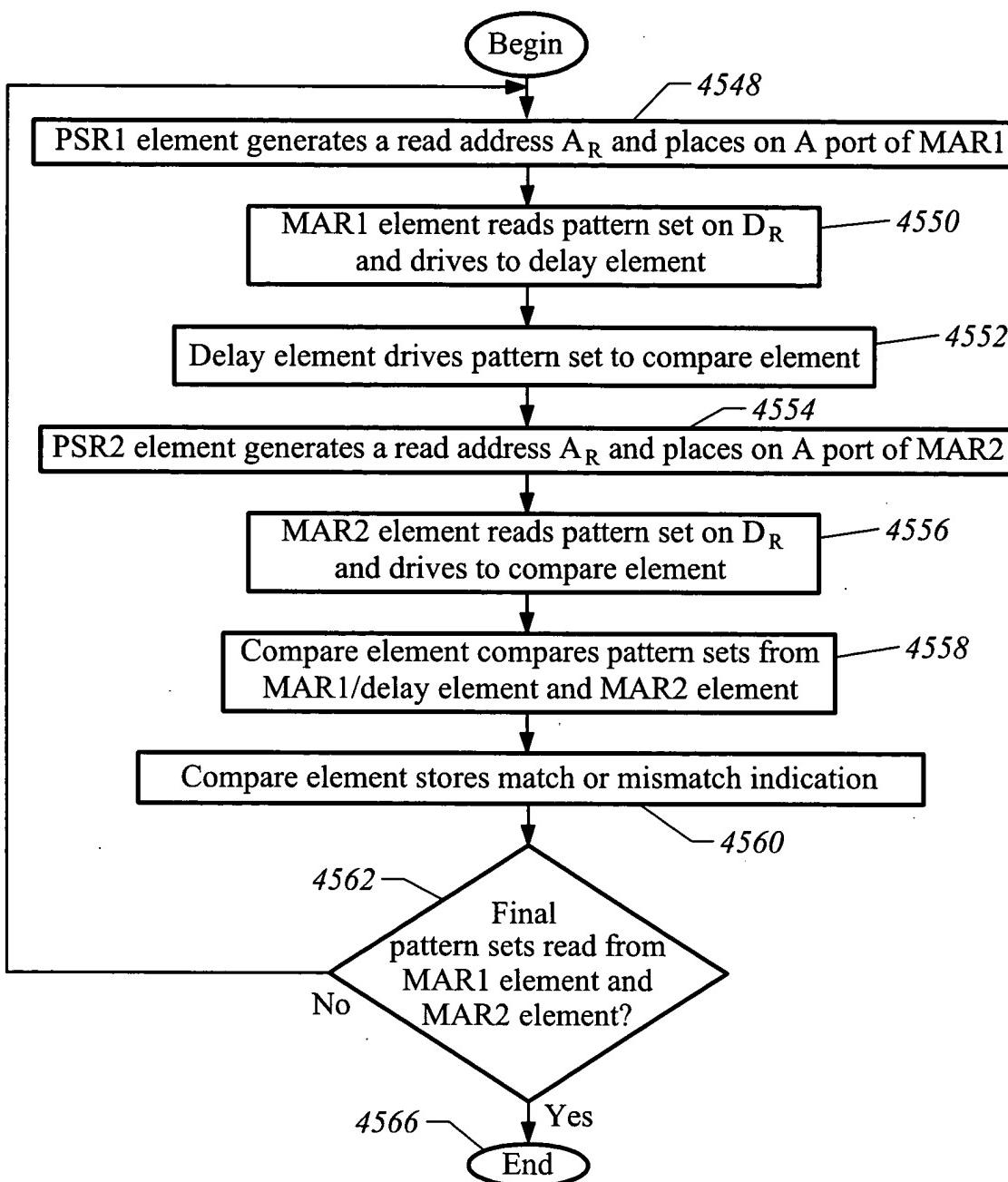


FIG. 45D

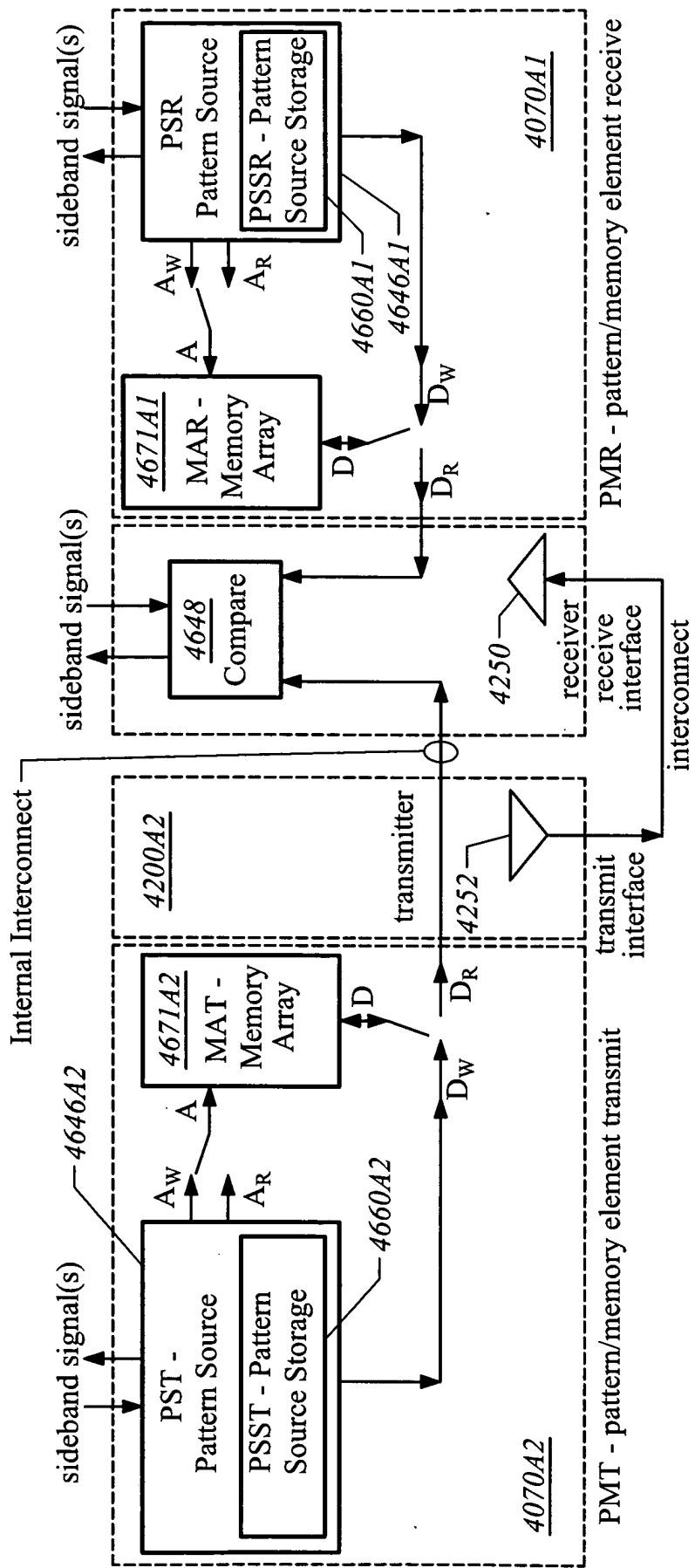
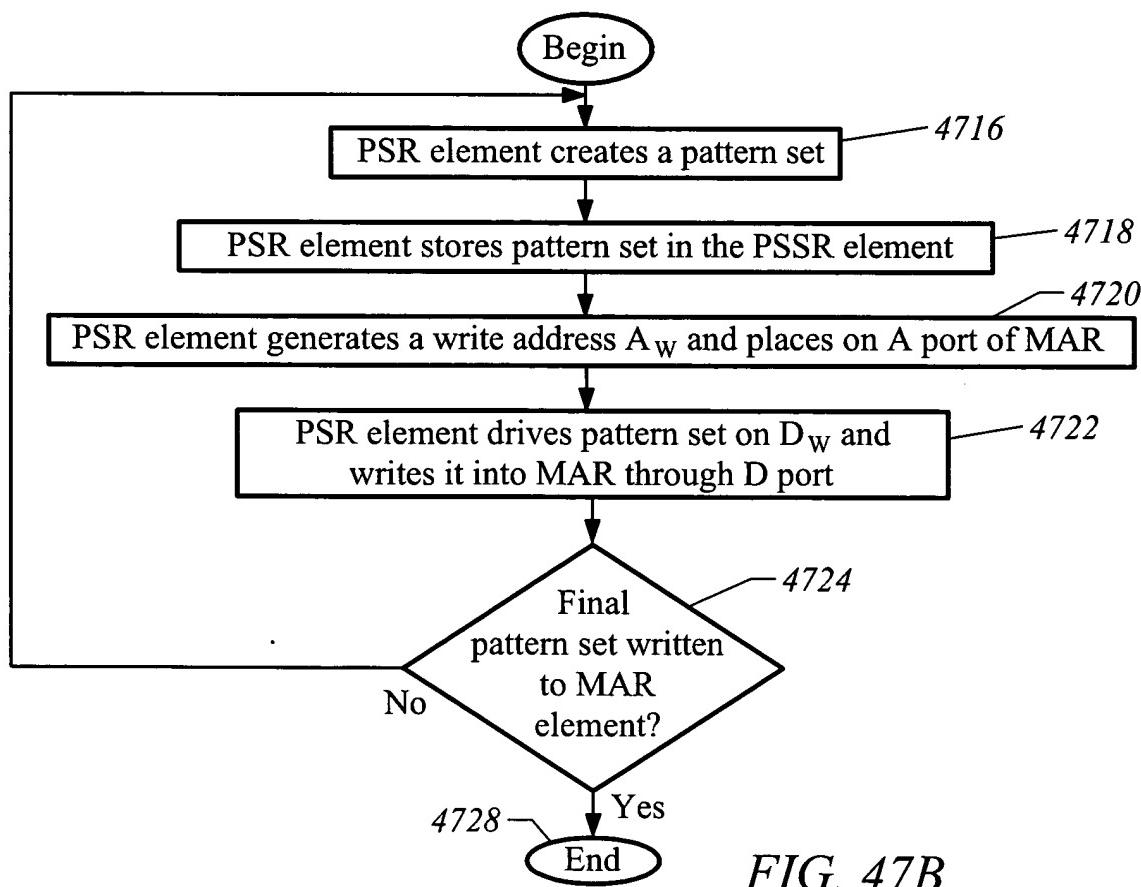
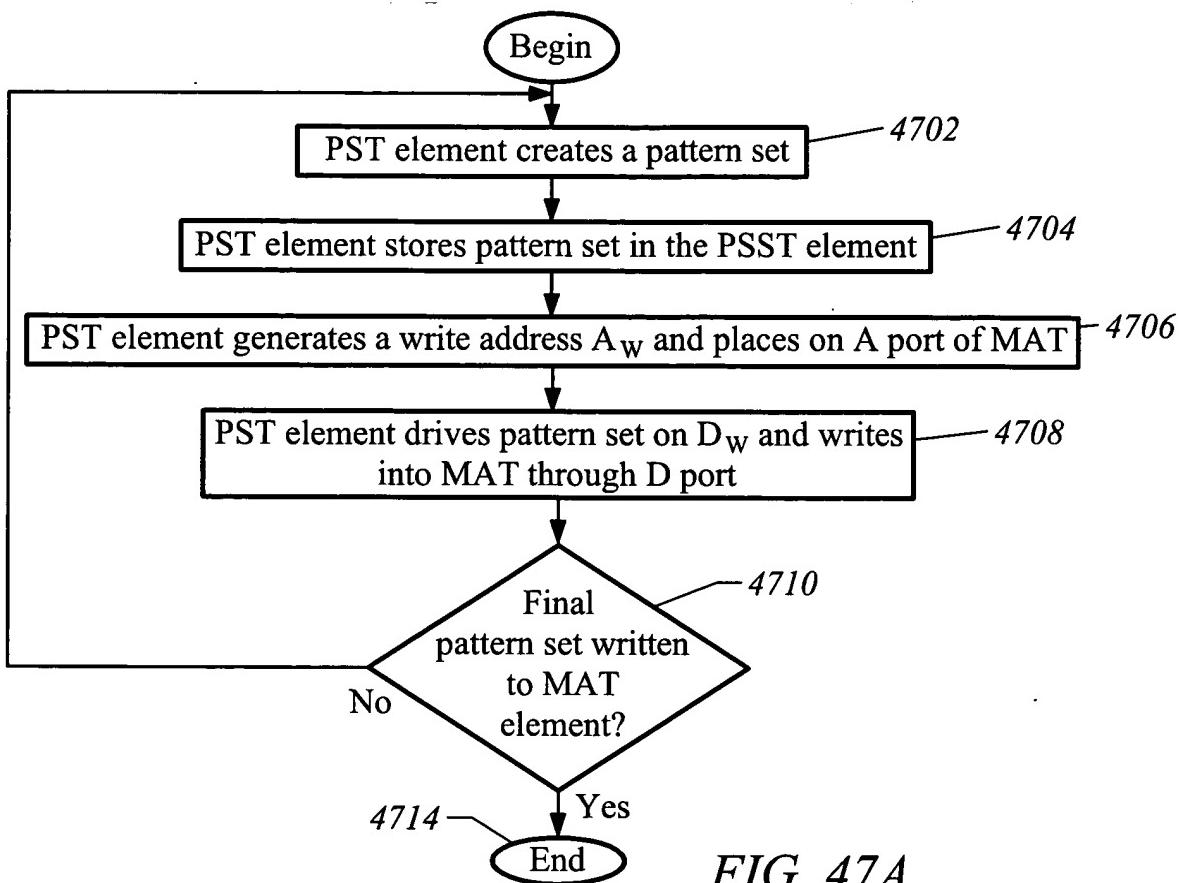


FIG. 46



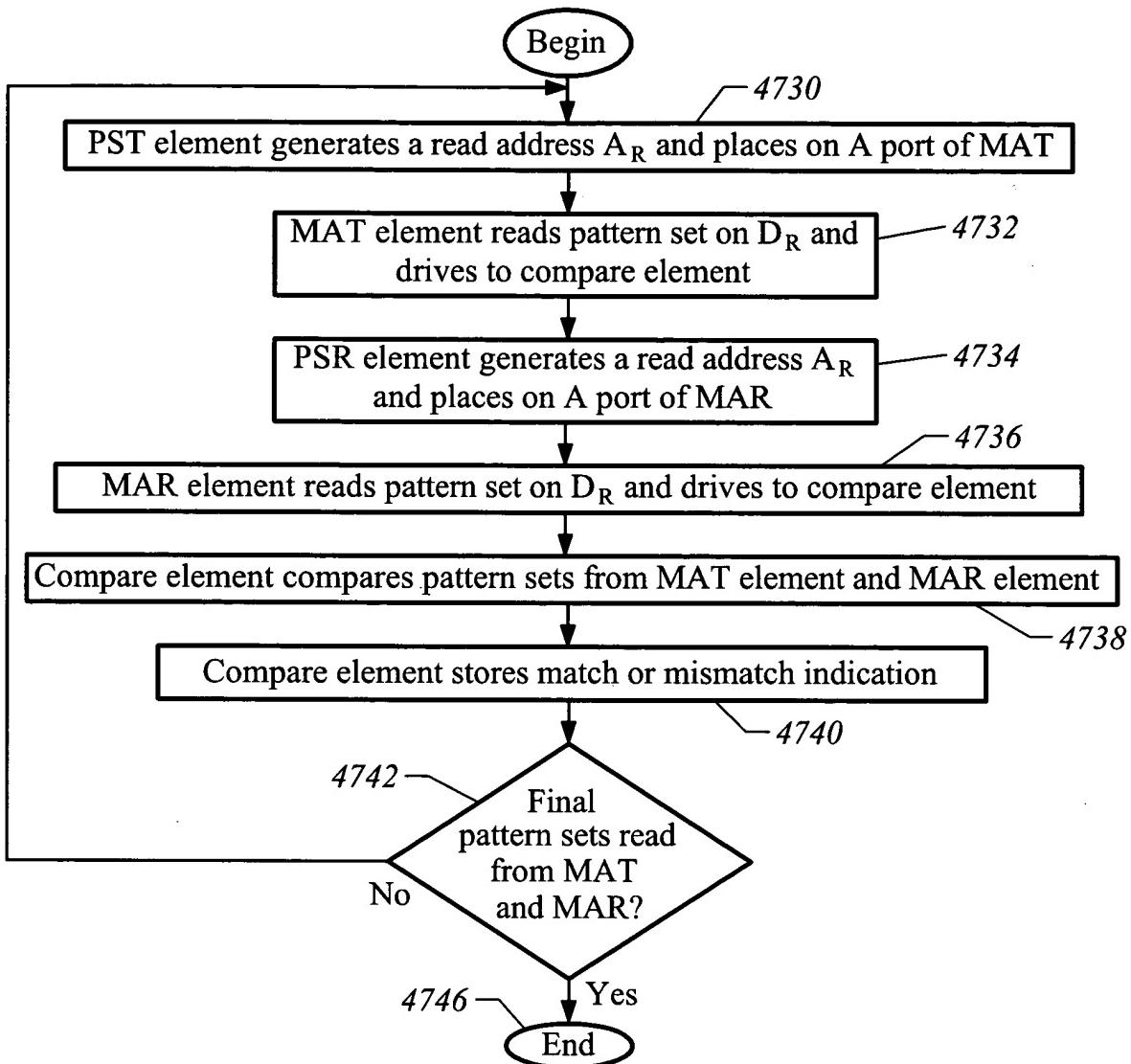


FIG. 47C